Pixel tracker for the Mu3e experiment

Ashley McDougall on behalf of the Mu3e collaboration

Silicon tracking and vertex detector technologies workshop

Queen Mary, University of London | 07.11.23

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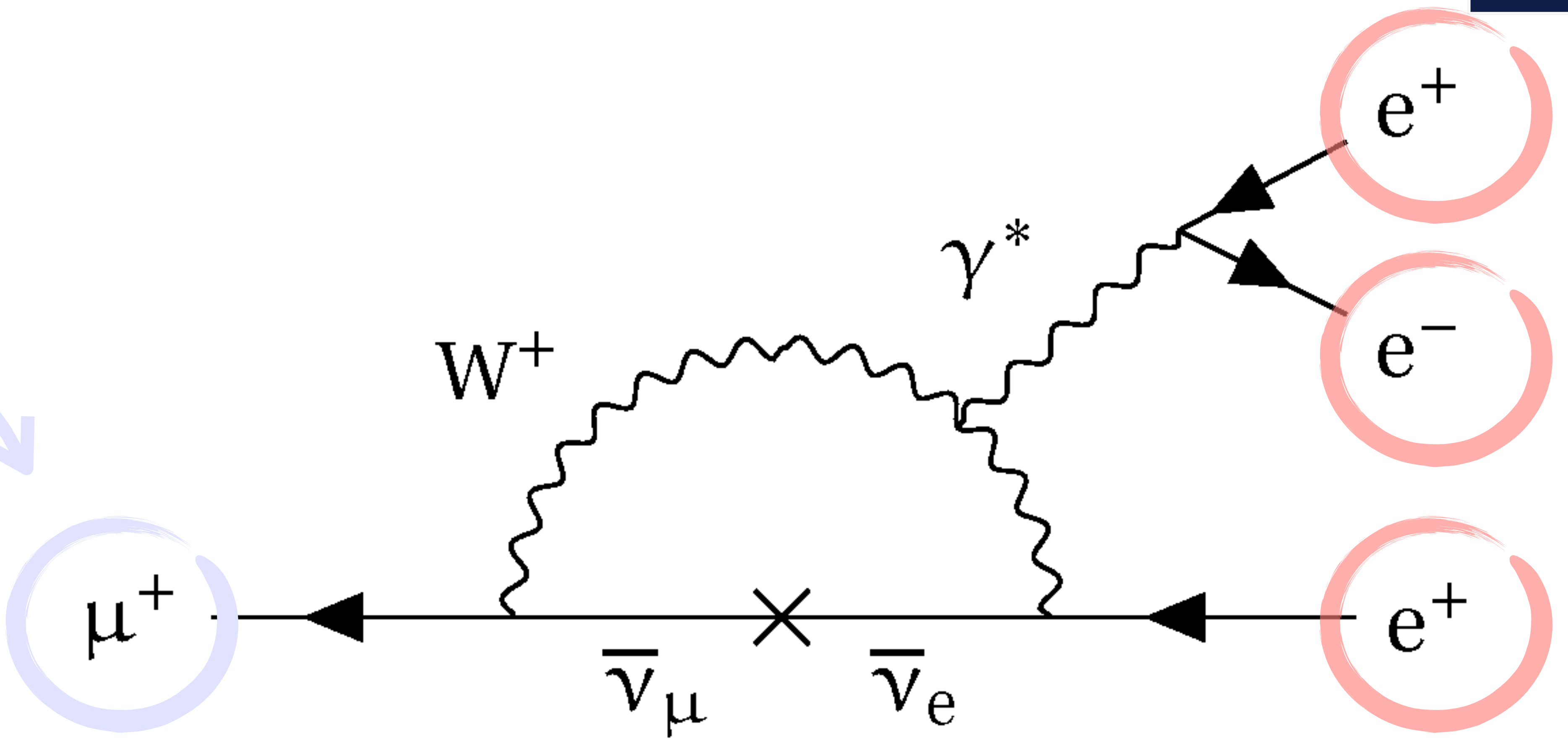
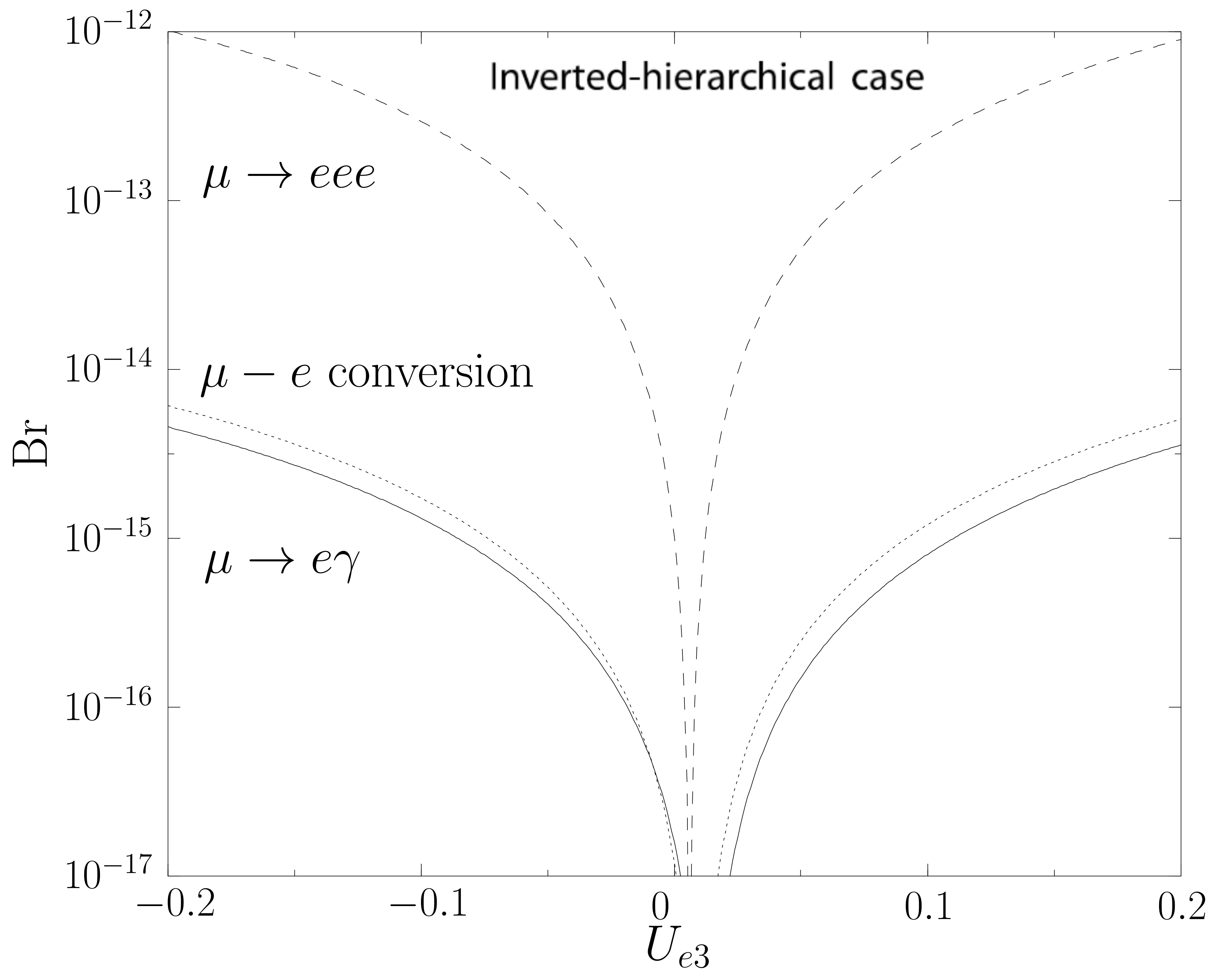
Aim to observe the process $\mu^+ \to e^+e^-e^+$



Lepton flavour violating decay in the SM

- Charged LFV decays forbidden at tree level (Induced through lepton mixing at higher orders)
- Predicted BR($\mu \to eee$) $\sim 10^{-55}$ [arXiv]

BSM models involving LFV could significantly enhance the predicted BR (e.g. triple Higgs doublet model)



Anticipated sensitivity BR($\mu \to eee$) $\sim 10^{-16}$

- Best current upper limit: BR($\mu \to eee$) < 10^{-12} @ 90% C.L. from SINDRUM (1988)

Complementary to other similar searches:

- Direct LHC searches
- Indirect searches of tau and other muon decays (Mu2e, MEG-II)

Experimental considerations:

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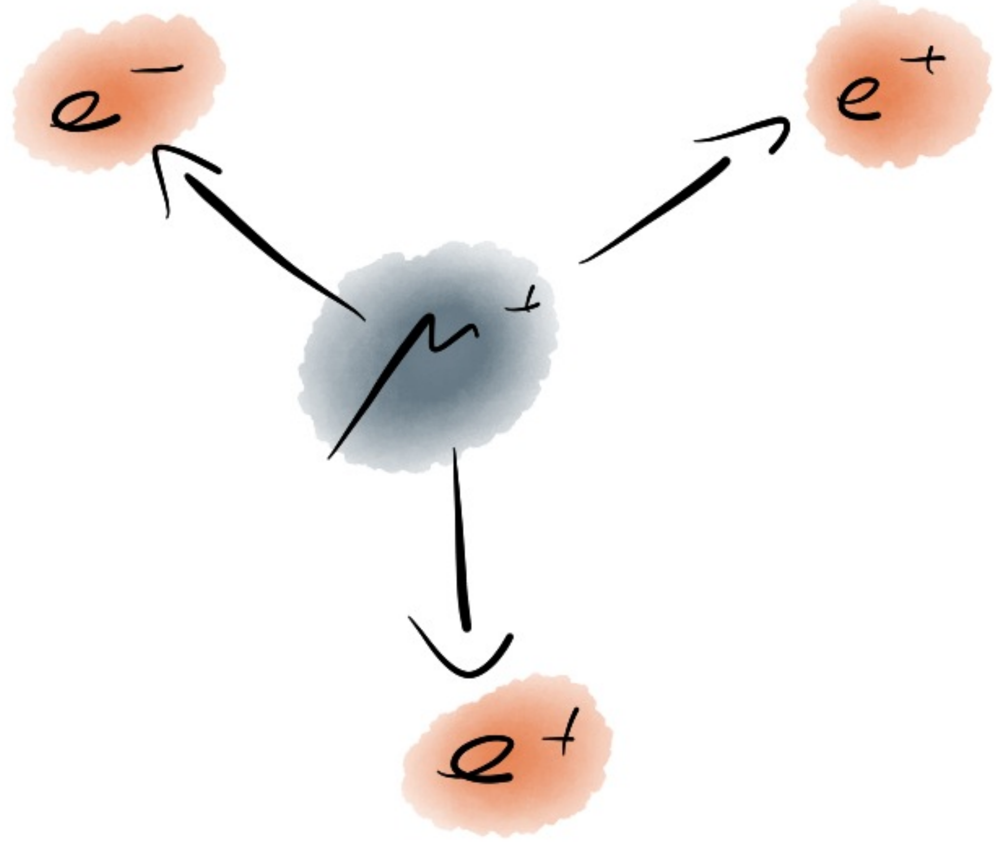
Signal topology: three electron tracks

- Common vertex
- Time coincidence
- Energy sum = m_μ
- Decay at rest so $\sum \vec{p} = 0$



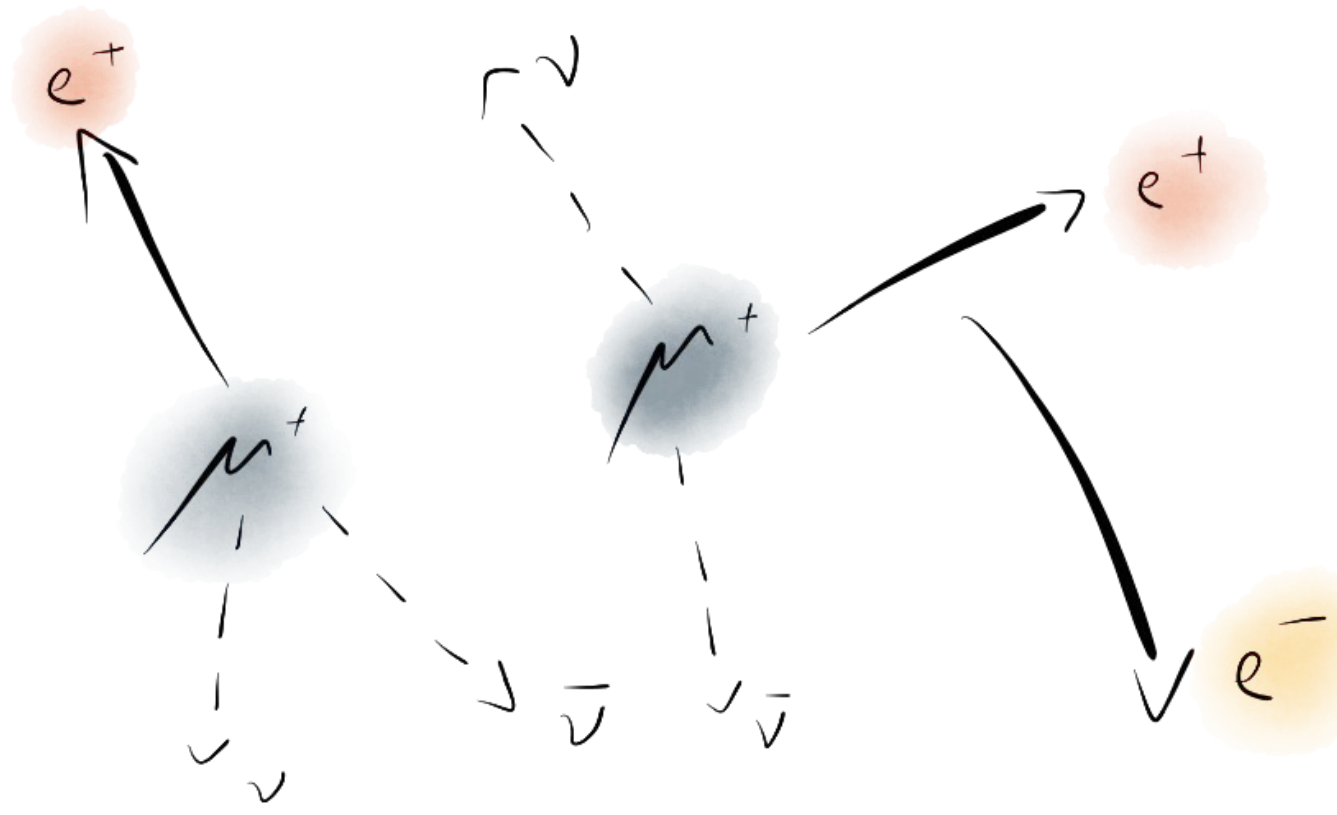
- Sensitivity dependant on reduction of dominant processes which resemble signal

Main backgrounds:

- Internal conversion (small energy carried away by neutrinos):

  BR($\mu \to eee\nu\nu$) = $(3.4 \pm 0.4) \times 10^{-5}$
- Accidental: processes appearing to have 3e tracks.

  Can occur via: Misreconstruction, γ conversion, Bhabha scattering



Detector requirements:

- Precise momentum resolution (***material budget important***!)
- Good timing and vertex resolution (to identify the signal)
- Large acceptance

Mu3e location and collaboration:

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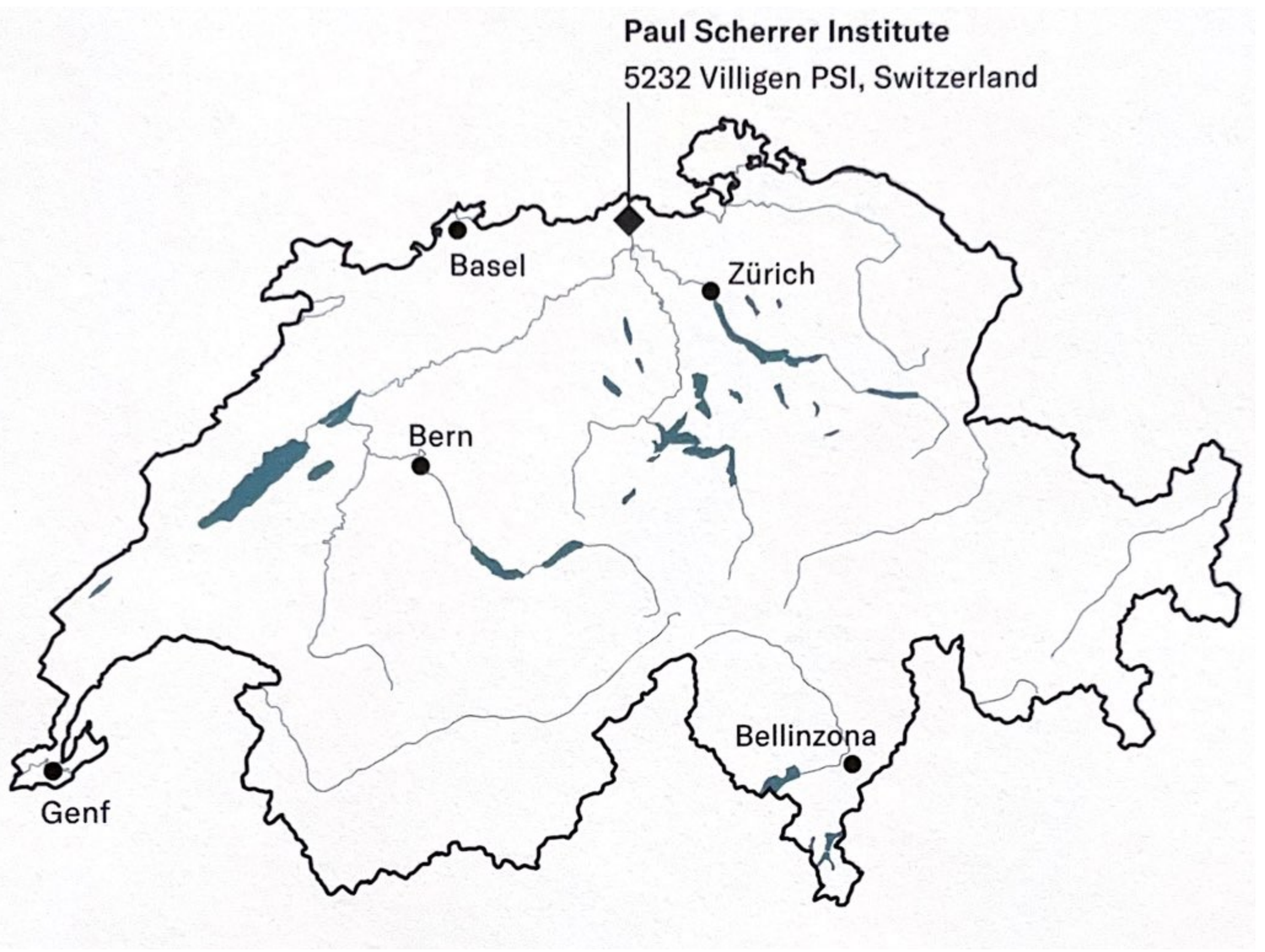
Located at the Paul Scherrer Institute (PSI) near Zurich, CH



- Swiss national accelerator complex
- Mu3e to be located in experimental hall along low-energy muon beam line
- Provides muon rates up to $\sim 1 \cdot 10^8$ Hz

Expected to start taking physics data in 2025:

- 290 days *minimum* running time required to achieve target sensitivity

Collaboration $\mathcal{O}$(80 people) from 11 institutes (Germany, UK, Switzerland):

PAUL SCHERRER INSTITUT PSI

ETH zürich

UNIVERSITÉ DE GENÈVE

Universität Zürich UZH

UCL

University of BRISTOL

UNIVERSITY OF LIVERPOOL

UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

UNIVERSITY OF OXFORD

KIT Karlsruher Institut für Technologie

JG|U JOHANNES GUTENBERG UNIVERSITÄT MAINZ

The Mu3e detector overview:

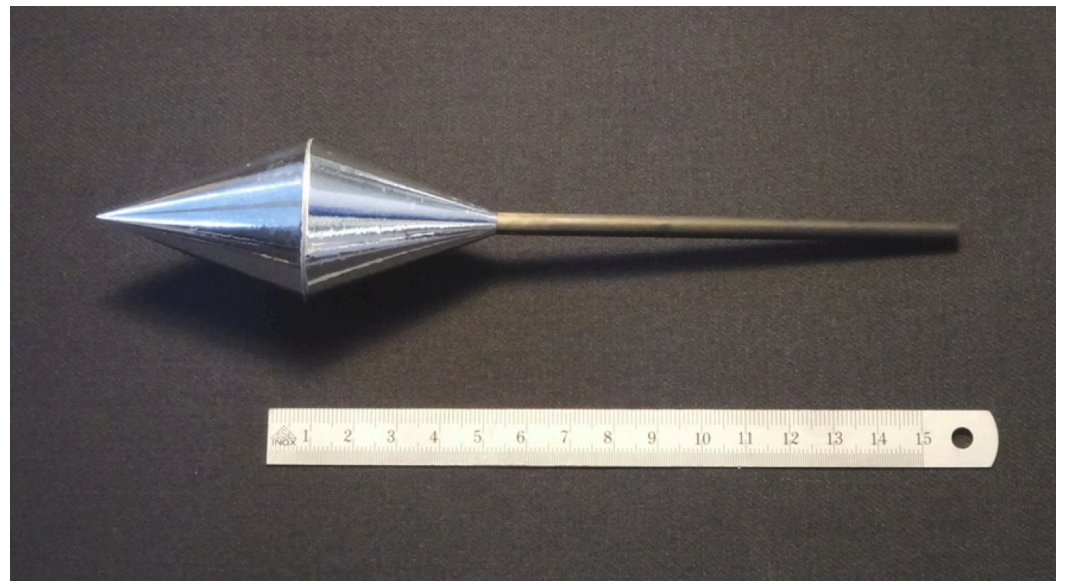
1 **Make muons**

- πE5 beam line @ PSI

2 **Stop the muons**

Hollow double cone stopping target:

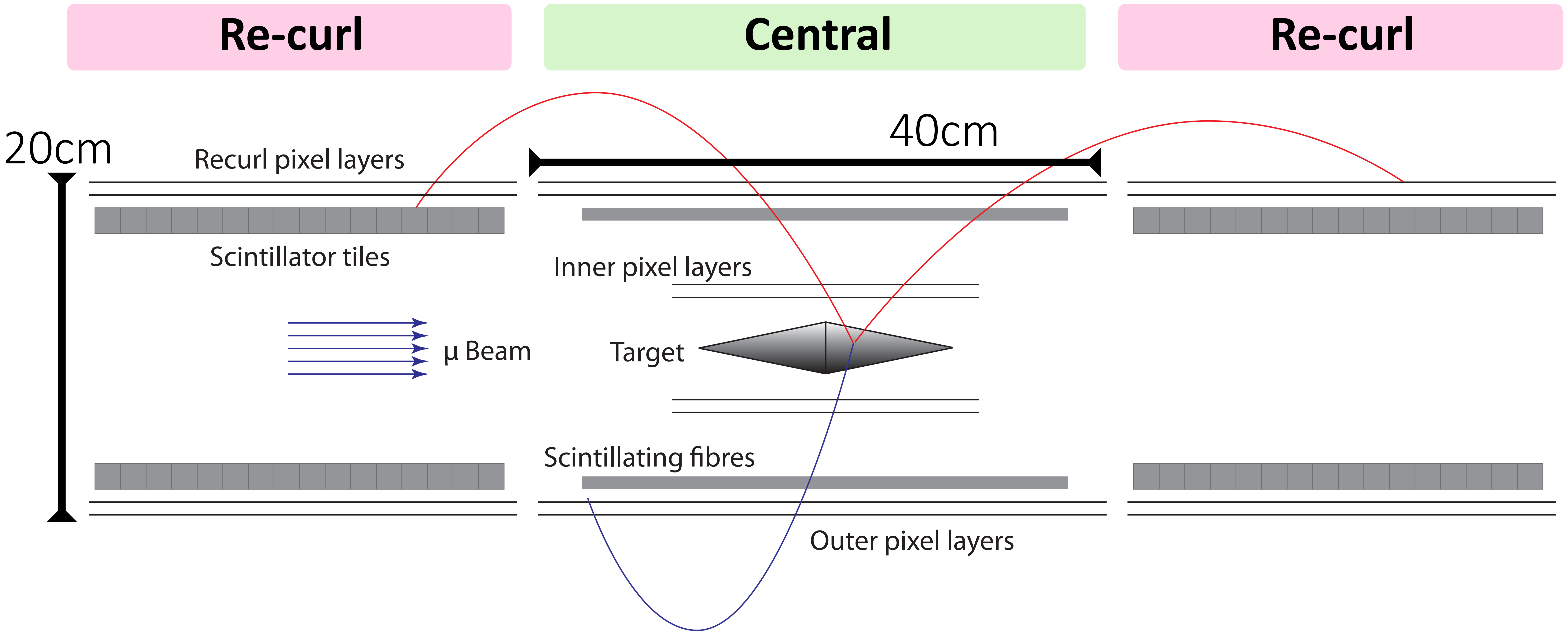
- Aluminised Mylar foil 70-80µm thickness, 100mm length, 19mm radius.
- ~ 95.5 % of muons reaching the target are stopped
- Very similar to that used by SINDRUM



3 **Detect the muons**

Detector geometry:

- **Central region**: pixel tracker + scintillating fibres
- **Re-curl region**: pixel tracker + scintillator tiles



Tracking achieved with:

- Homogeneous solenoidal magnetic field B = 1T
- Four-layer silicon pixel detector (+ re-curl)
- Scintillating fibres: differentiate electrons and positrons
- Scintillating tiles: further improve timing resolution

Detector requirements:

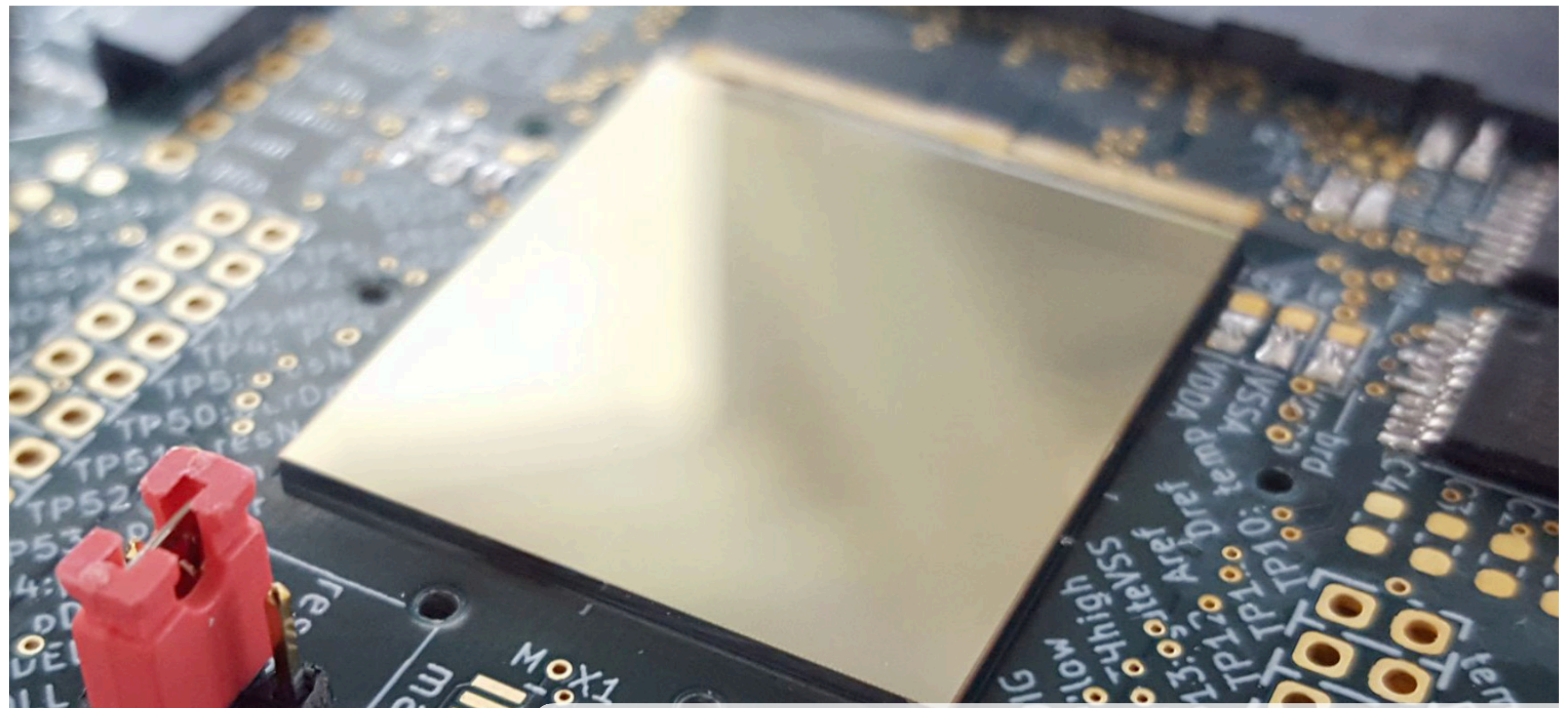
Require excellent momentum (energy) resolution to reduce $\mu \rightarrow eee\nu\nu$ background

- Small pixel sizes = hit resolution effects can be neglected.
- **Resolution solely determined by multiple scattering.**
  In such a regime: **track momentum resolution predominantly depends on number of detector layers & thickness.**

Maximise resolution = *ultra low-mass* detector!

For tracking:

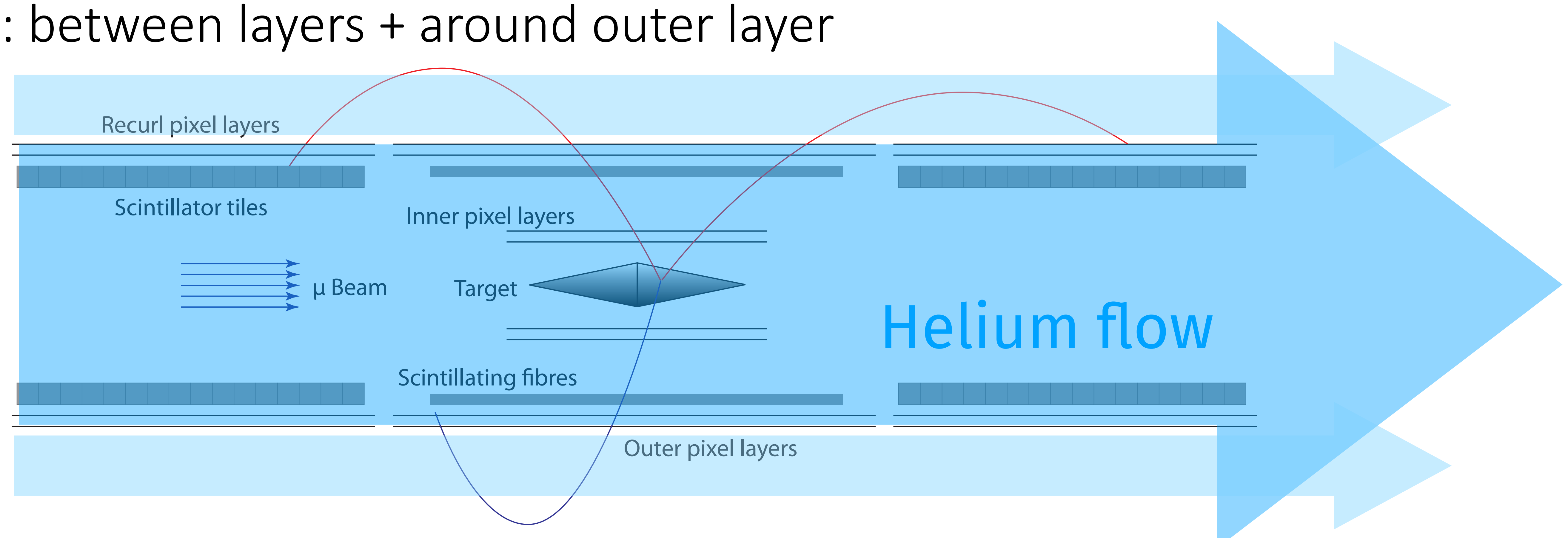
- Use very thin (50-70μm) pixel sensors, with integrated hit digitisation and readout circuitry



MuPix silicon pixel chip

Cooling: use gaseous Helium cooling

- 2 flow channels: between layers + around outer layer
- Flow rate 2g/s



Scintillating fibres and tiles:

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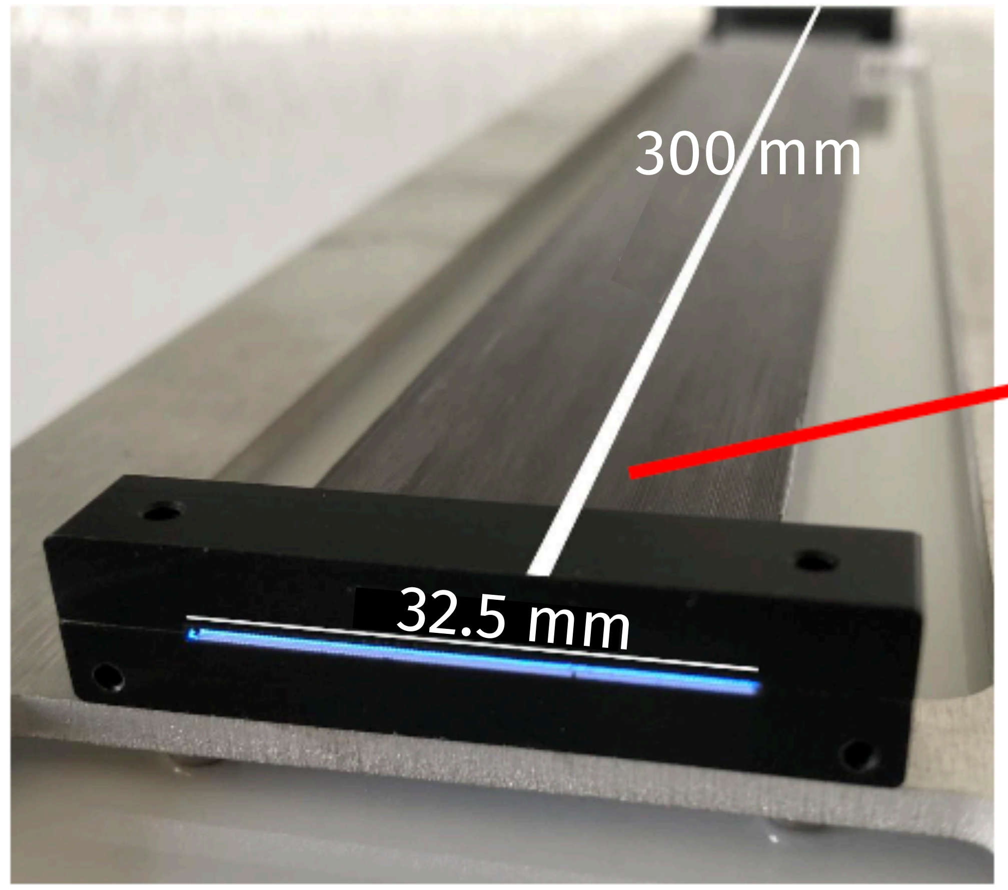
Scintillating fibres: surround inner pixel layers in central region

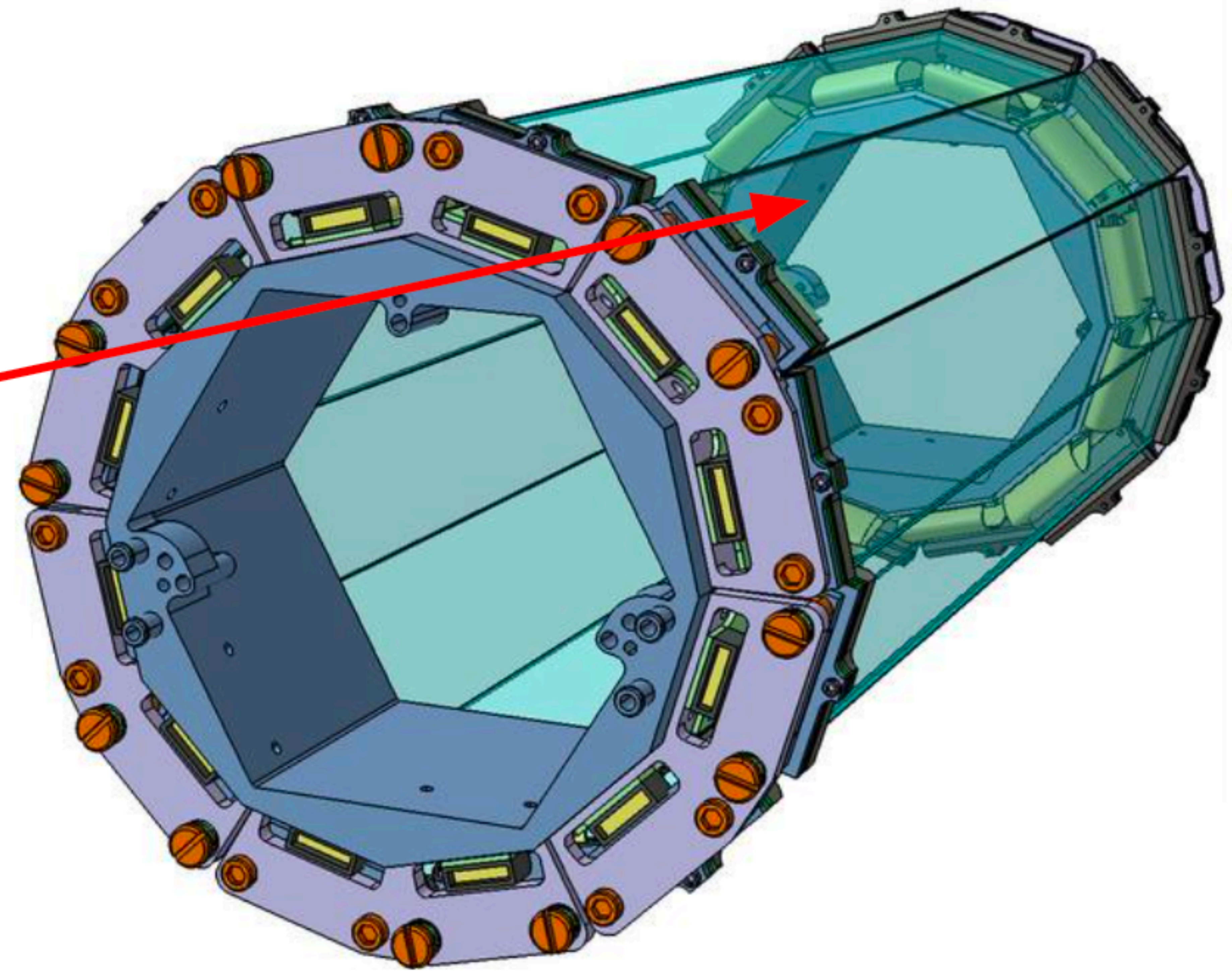
- Constructed of scintillating photo-multiplier tubes (SiPMs)
- 12 fibre ribbons, 30cm long, arranged in 3 staggered layers
- Fibres 250 µm thin
- Material budget < 2% X_0
- Measured time resolution $\sim$ 250 ps

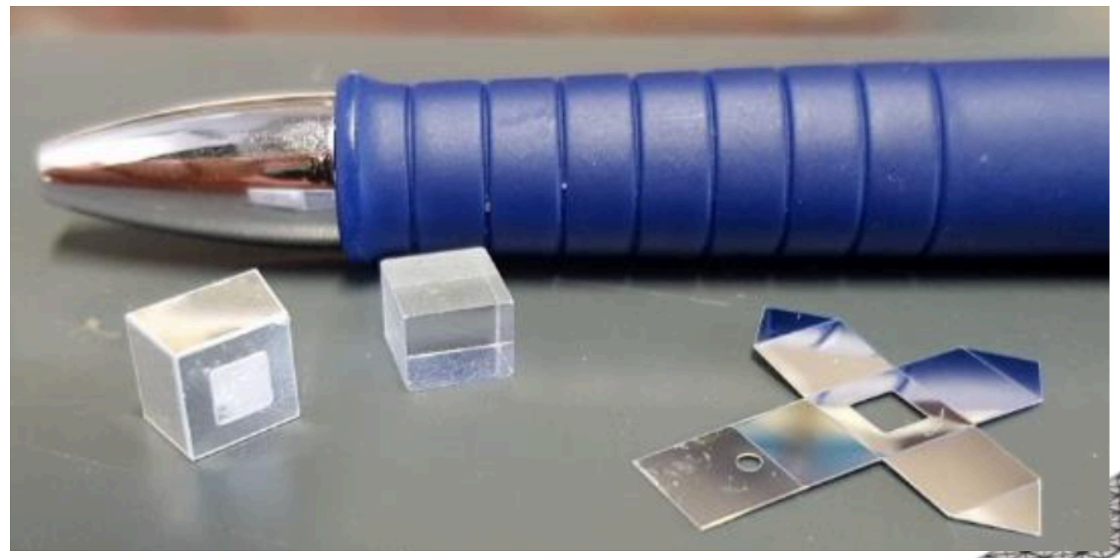
Scintillating tiles: 6mm x 6mm x 5mm tiles with SIPMs in re-curl region

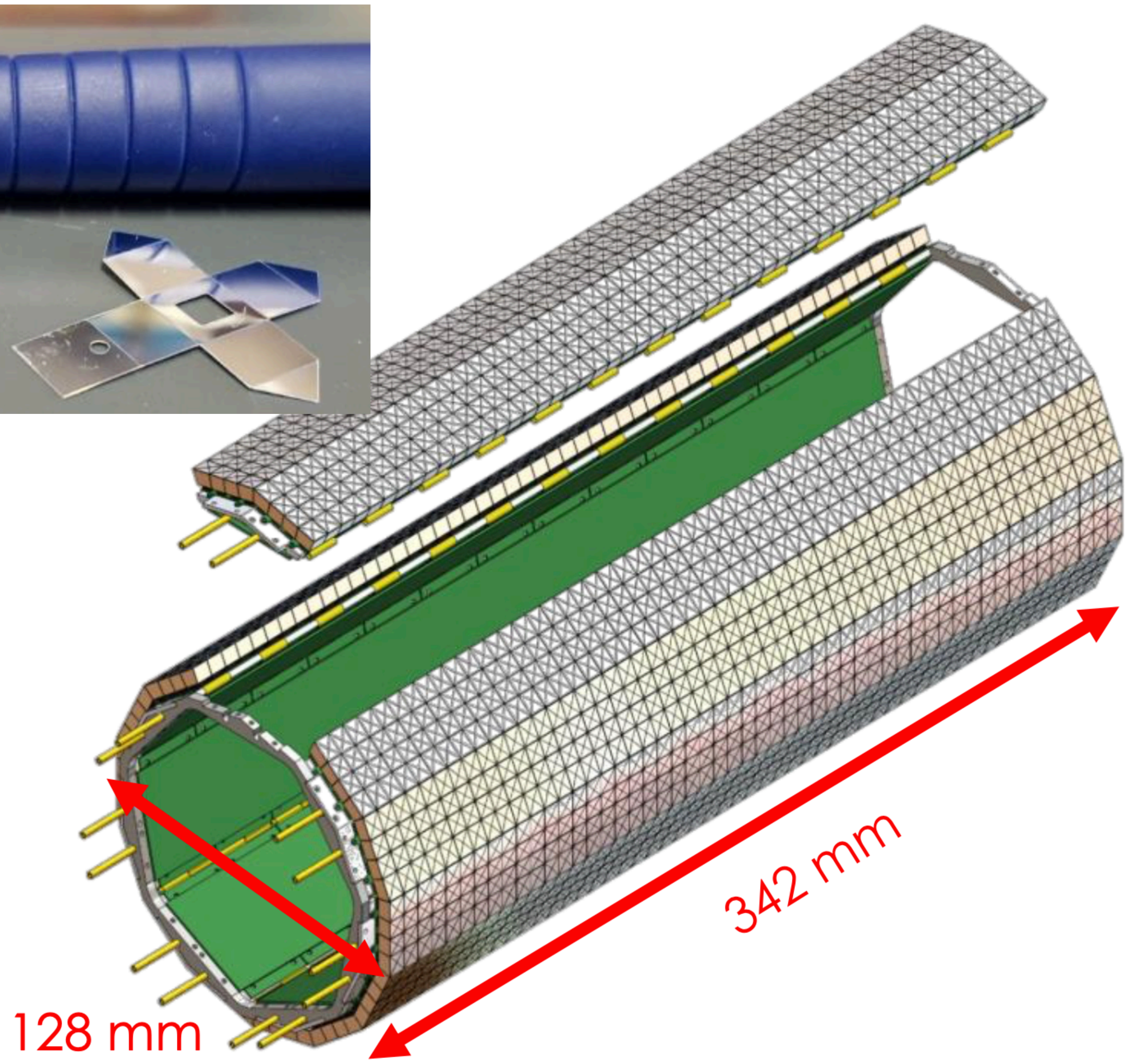
- $\sim$ 6000 channels
- Up to 60 kHz/channel
- Measured single channel time resolution < 50ps
- Intended to stop the electrons: no required material budget



SciFi ribbons







- Common read out: custom MuTRIG ASIC (50ps time-to-digital converter)

Pixel tracker for Mu3e:

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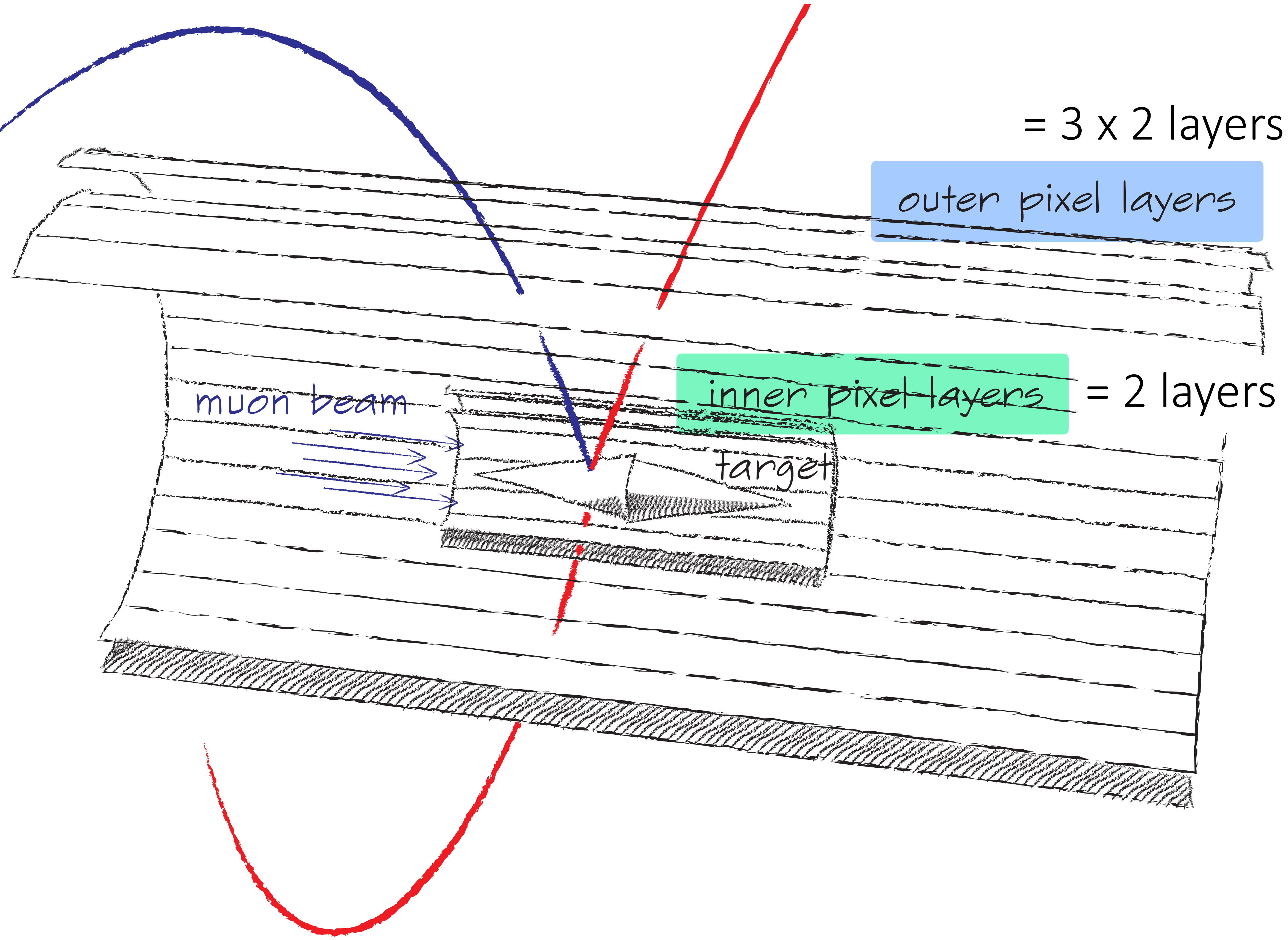
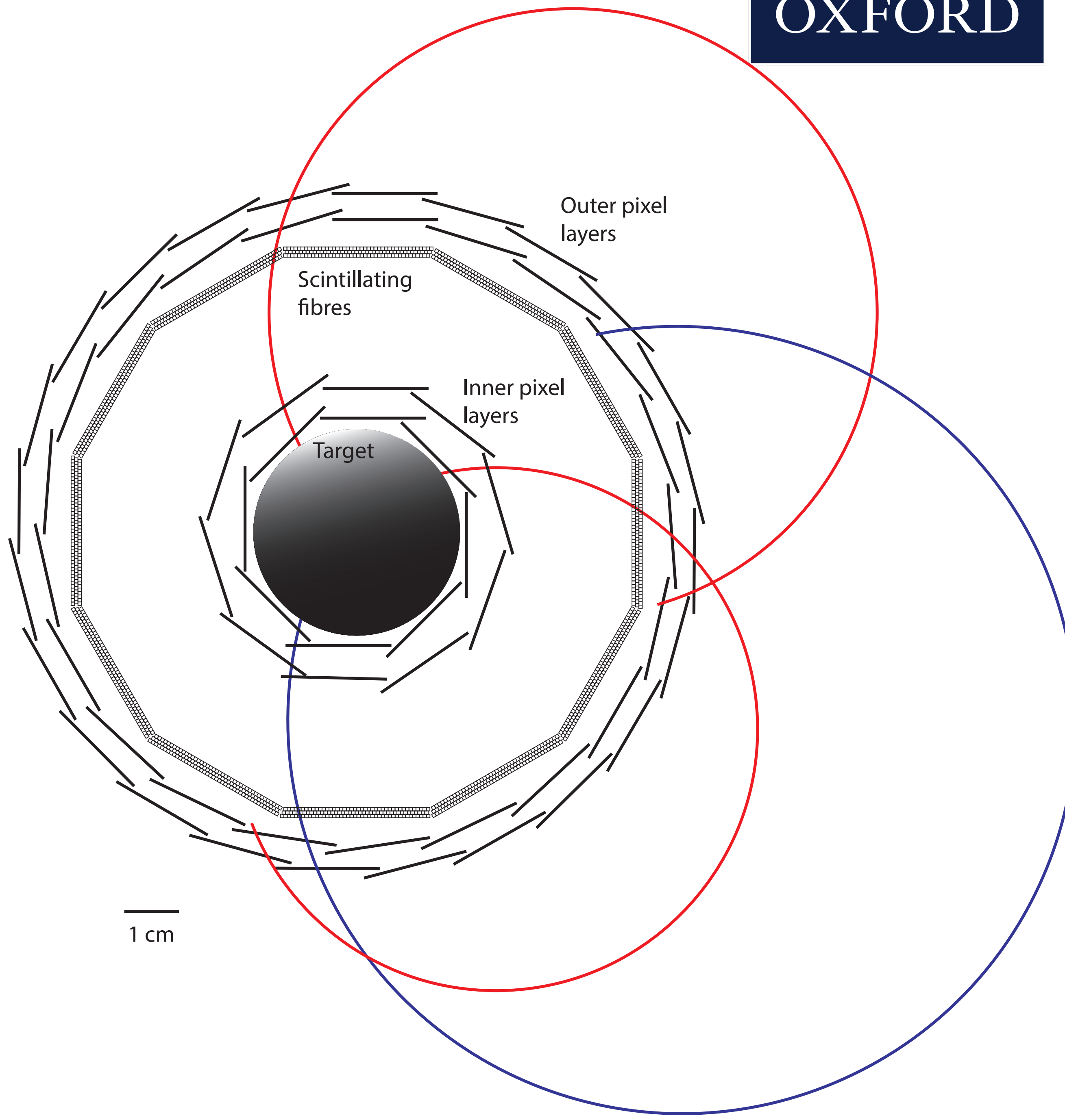
Silicon pixel detectors using **high-voltage monolithic active pixel sensor** technology (HV-MAPS)

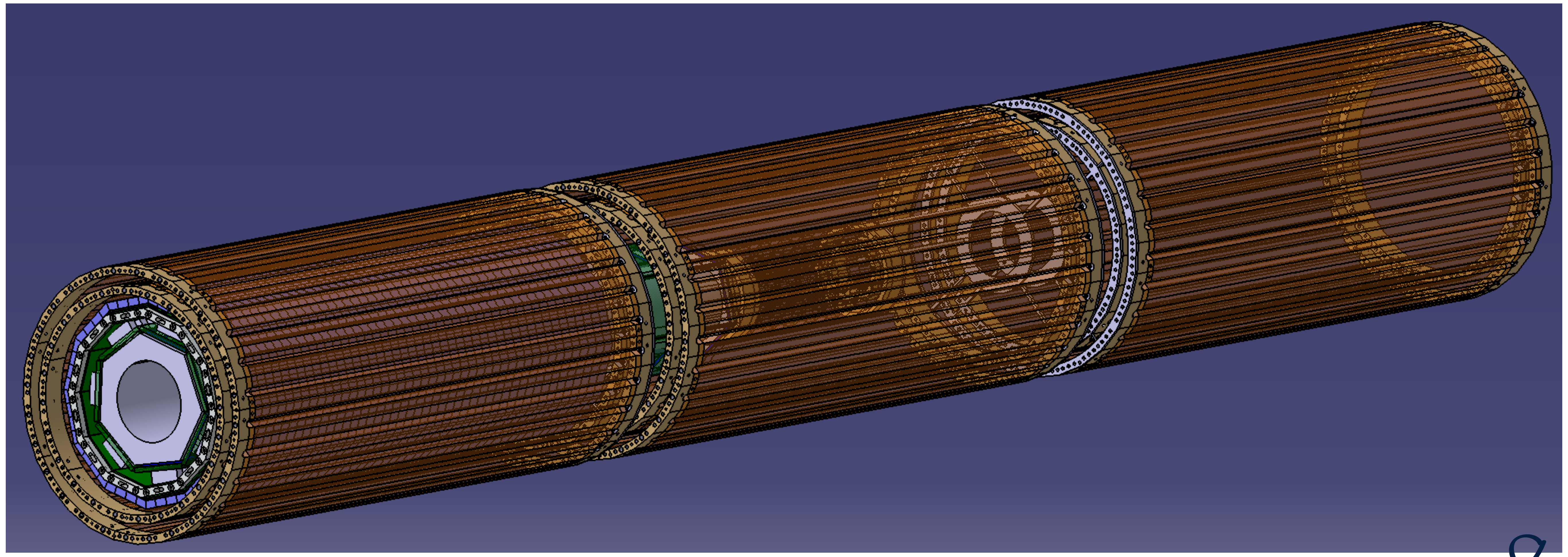
- Provides high granularity (precision tracking and vertexing)
- Needs to be **fast** and **accurate**



Ideal sensor design requirements

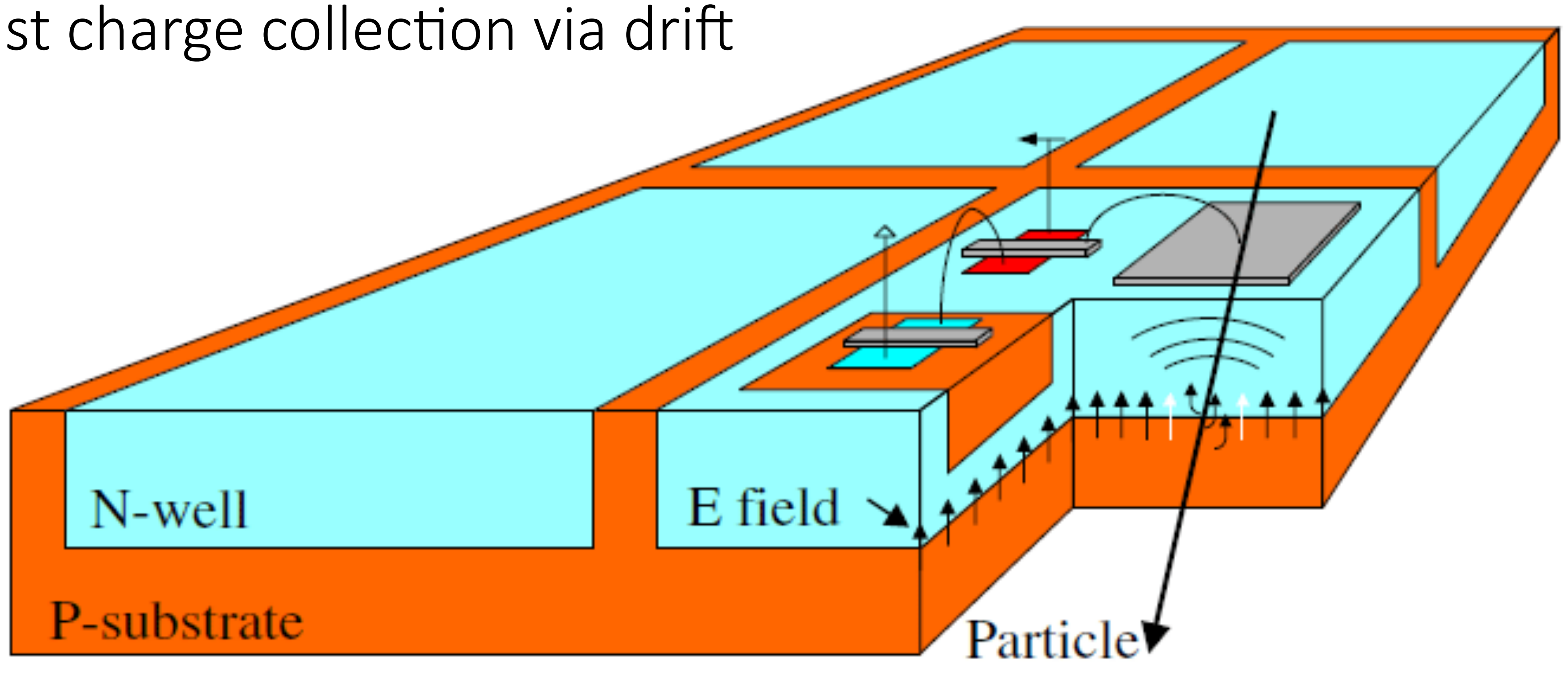
spatial resolution µm	≤ 30
time resolution [ns]	≤ 20
hit efficiency [%]	≥ 99
#LVDS links (inner layers)	1 (3)
bandwidth per link [Gbit/s]	≥ 1.25
power density of sensors [mW/cm^2]	≤ 350
operation temperature range [°C]	0 to 70



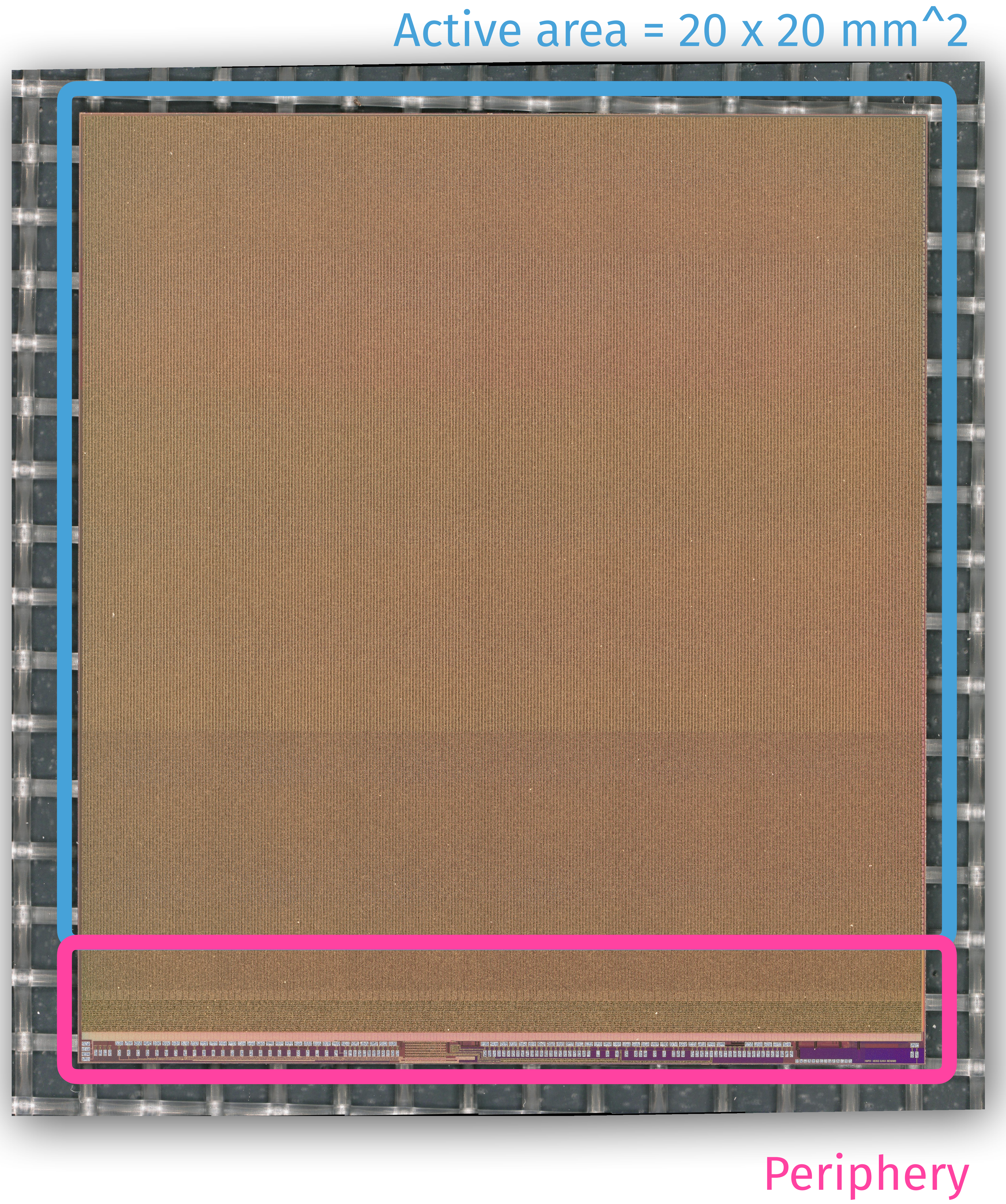


Custom **MuPix HV-MAPS** sensors: designed to be fast, efficient, thin

- Monolithic HV-CMOS: produced by TSI (Bosch) using 180 nm technology
- Fast charge collection via drift



- 80 x 80 μm^2 pixels (= 256 x 250 pixels total)
- Operating voltage = 1.8 V
- $\sim$ 250 mW/cm^2 power consumption
- < 15 ns time resolution (measured 5.7 ns)
- Tunable threshold for each pixel
- Integrated analog and digital readout
- Up to 3 configurable data lines: each at a rate of 1.25 GBit/s
- Data driven readout - hits sent out as packets



Inner pixel layers:

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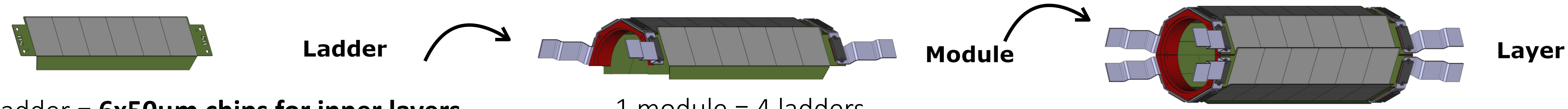
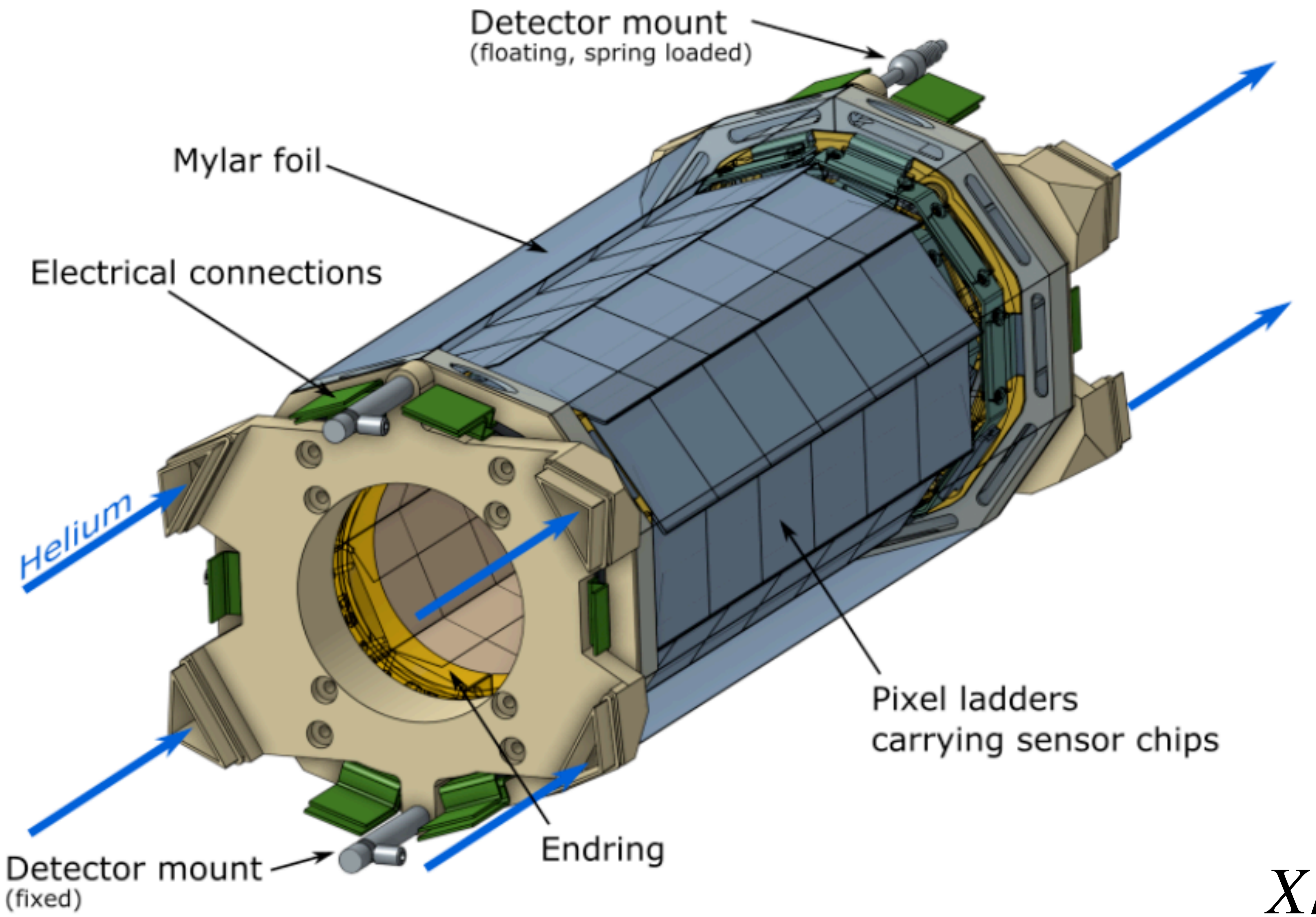
Chips assembled into **ladders**:



1 ladder = **6x50µm chips for inner layers**

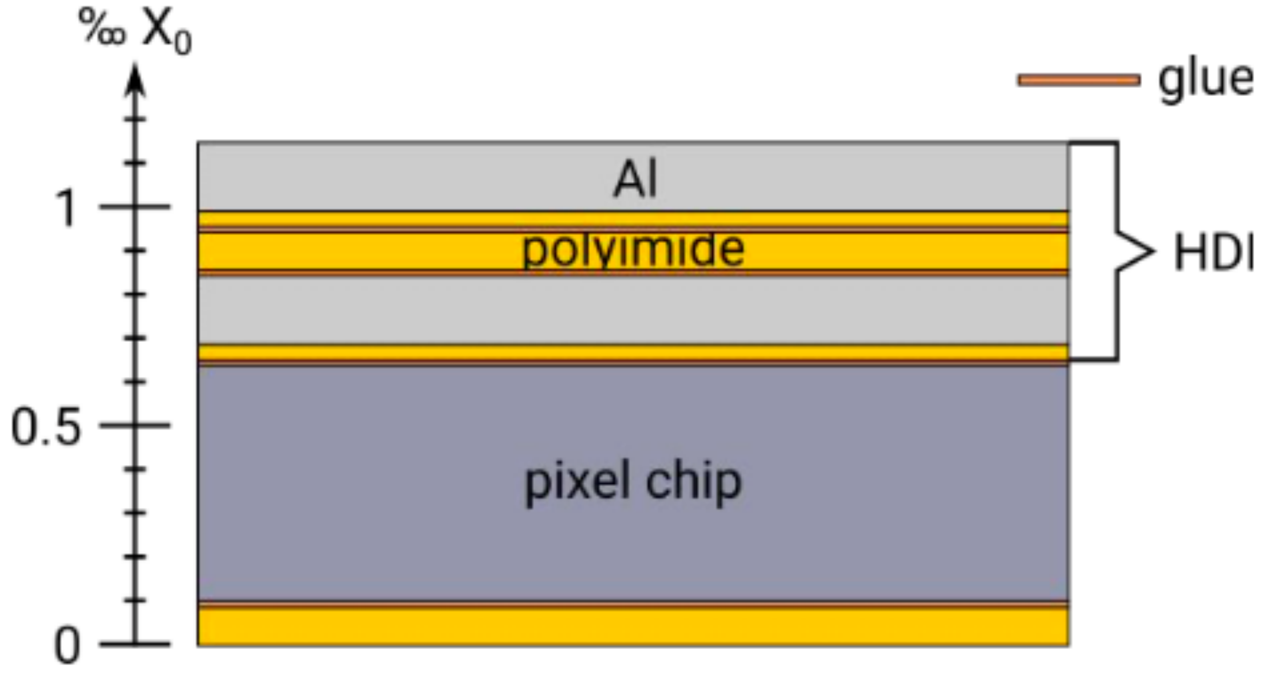
1 module = 4 ladders

2 modules = 1 layer



Mechanical support provided by:

- **Primarily from 3D folded nature of vertex detector**
- Alu/kapton high-density interconnect (HDI)
- Chips glued on + spTAB for electrical connection (Single Point Tape Automated Bonding)
- 25µm kapton support



$X/X_0 \approx 1.15\%$ per tracking layer

SpTA-Bond connection: bond pads size 200 x 100 µm^2

Fabrication procedure for inner pixel layers:

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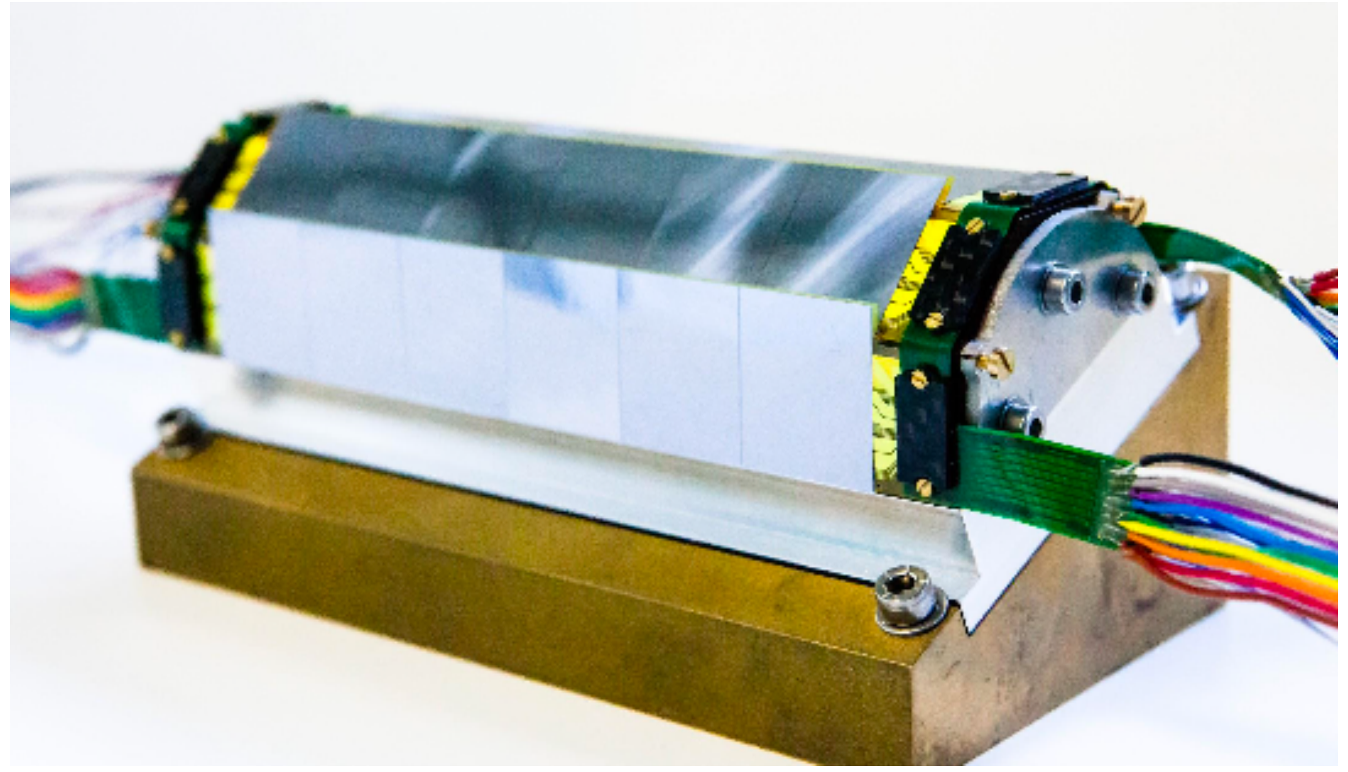
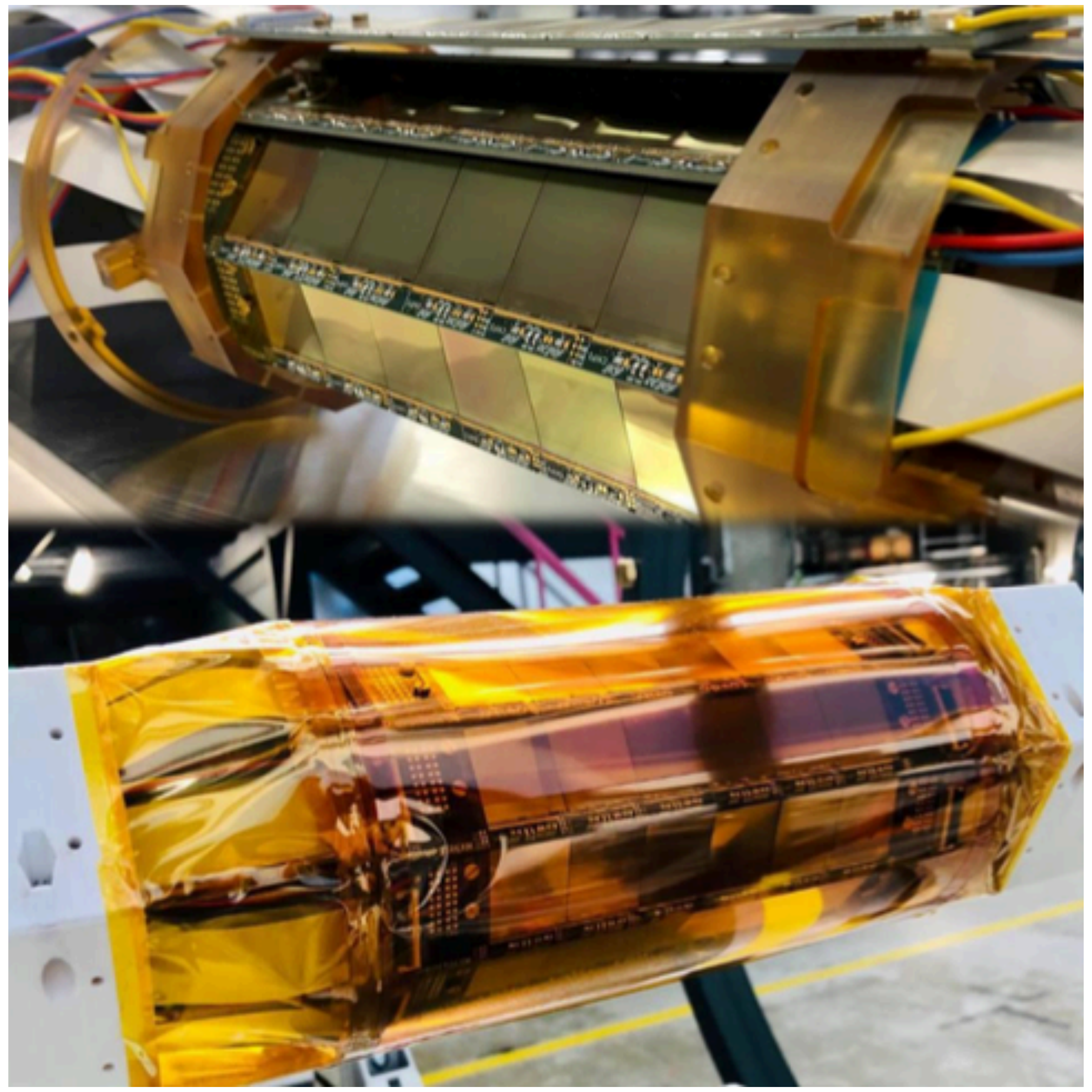
Test modules have been produced to conduct cooling studies, and practise assembly procedure



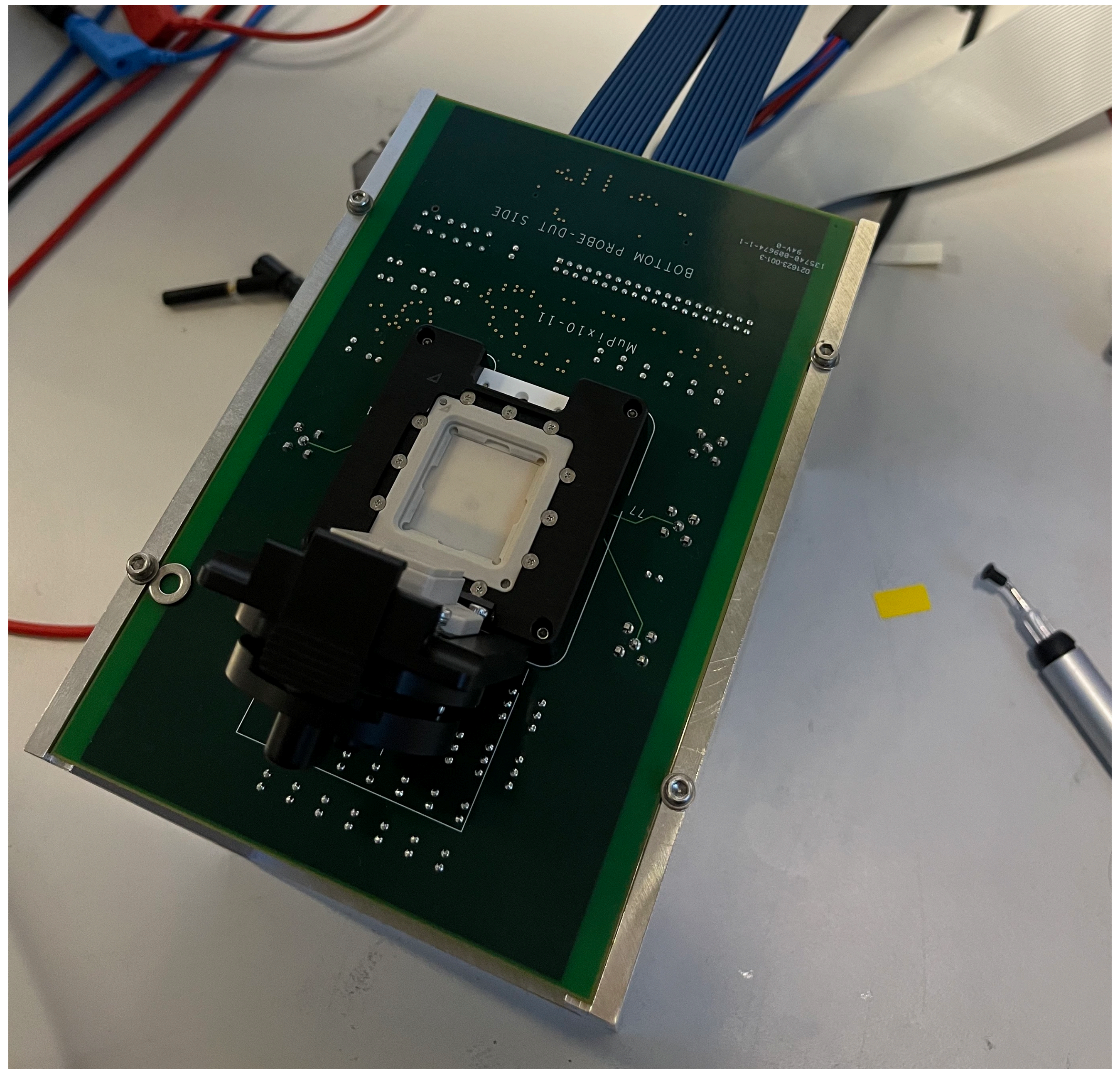
Simplified PCB-based demonstrator:

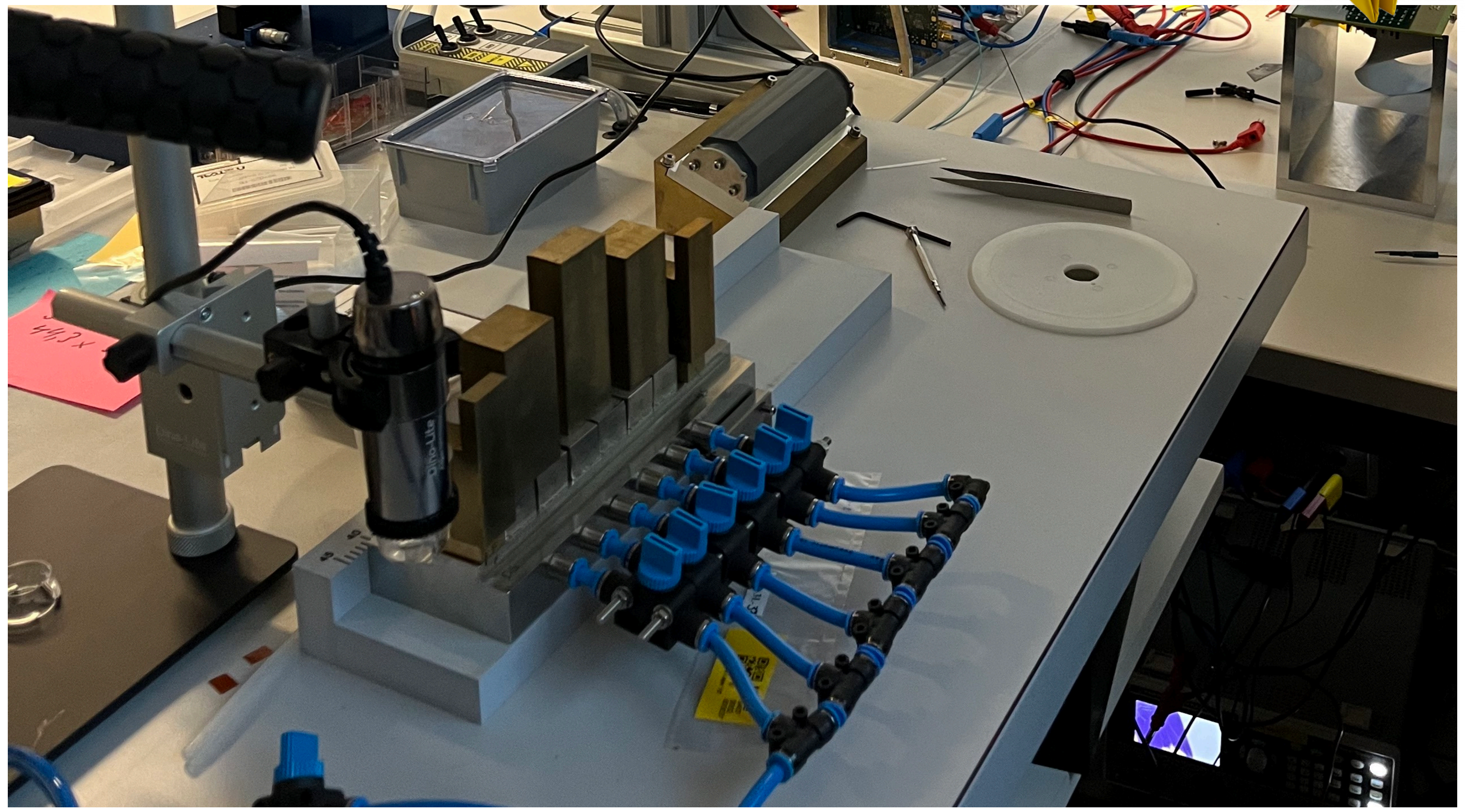


Single chips are tested using QC test stand with needle socket

Glue and chips place manually on ladder

- Some Origami skills required





First half ladder inserted into testbeam @ PSI 2 weeks ago

→ **operated in realistic beam conditions!**

Outer pixel layers:

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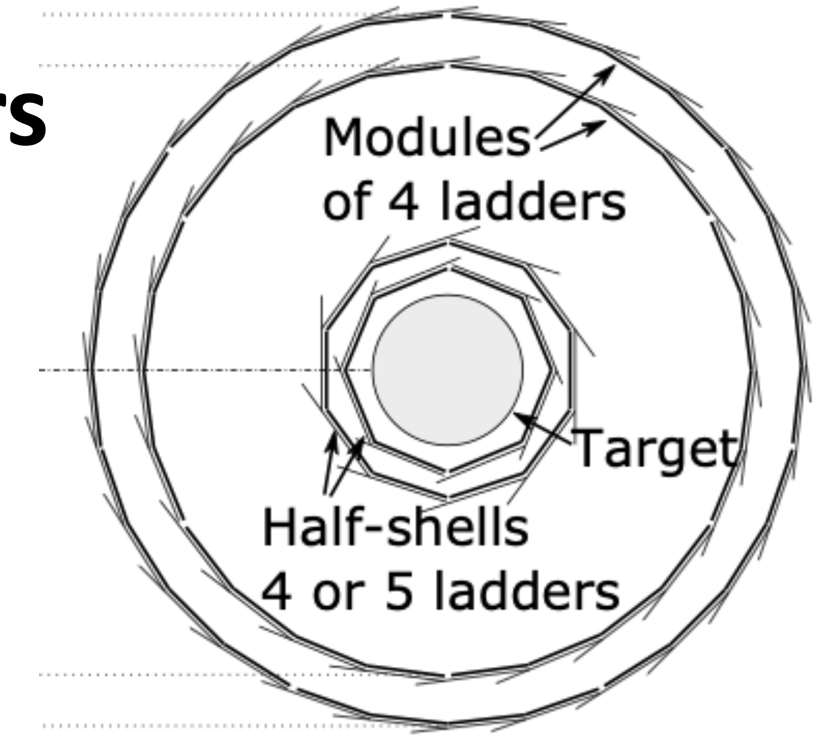
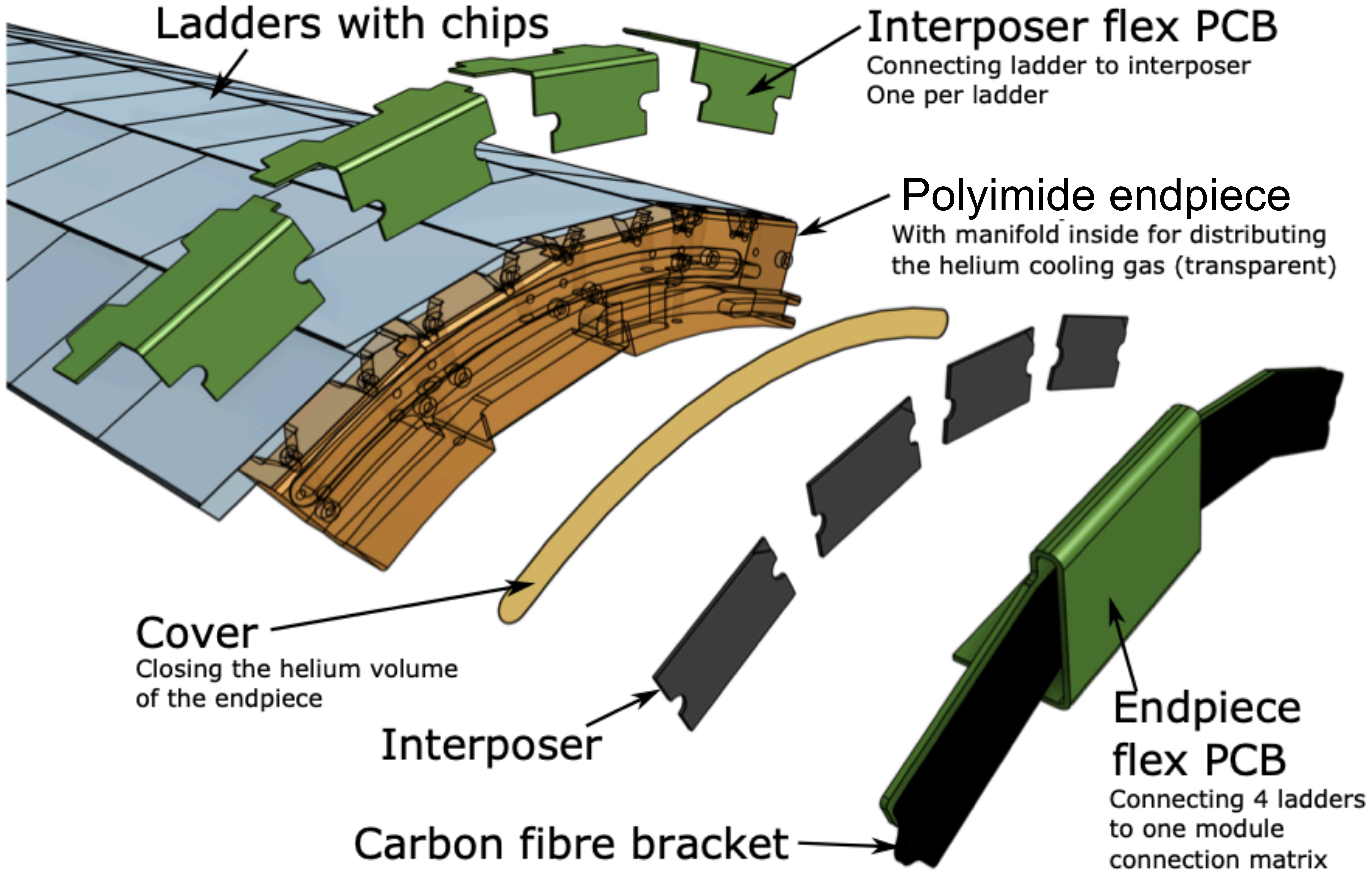
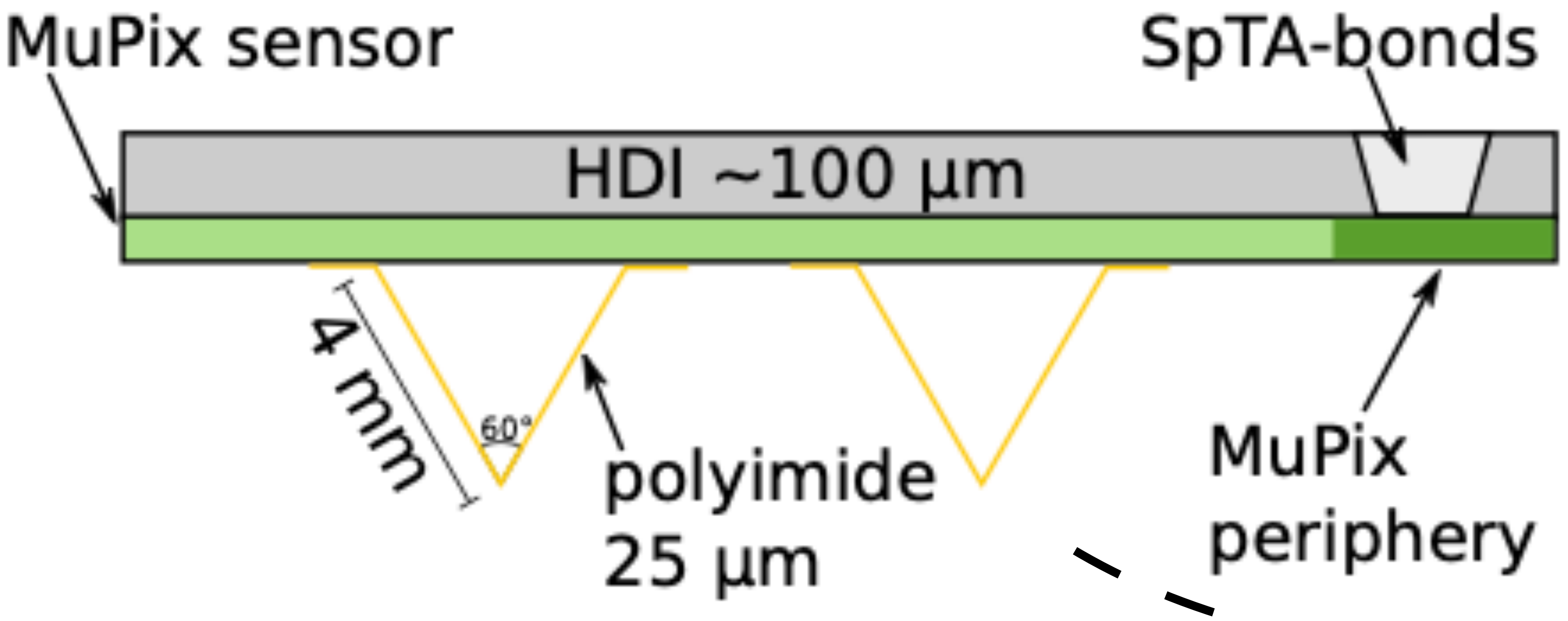
- **70µm thick pixel sensors**
- 17-18 chips per ladder
- 4 ladders per module
- 6 modules in layer 3
- 7 modules in layer 4



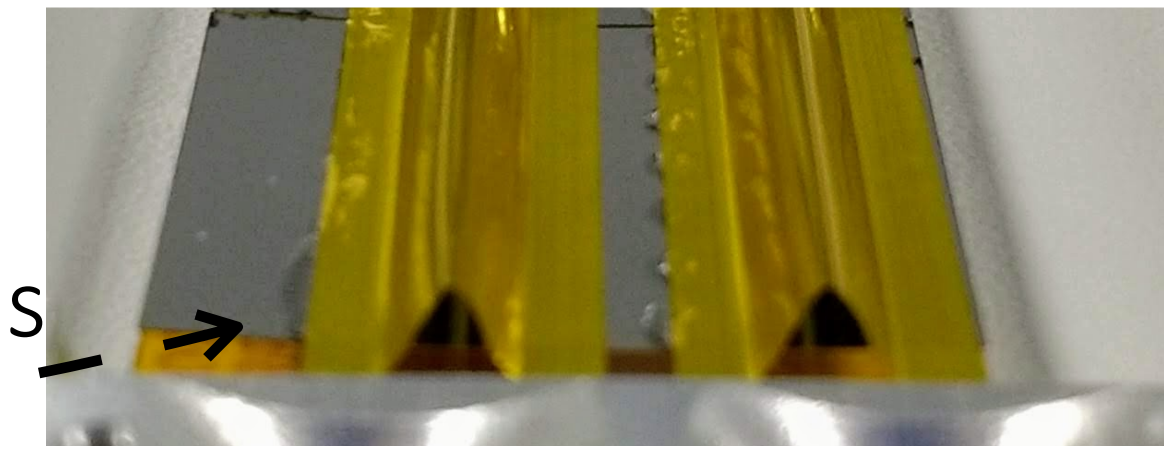


Mechanical support provided by:

- So-called “**v-folds**”: V shaped material providing structural rigidity (nominally made of kapton)



Real
v-folds



Fabrication procedure for outer pixel layers:

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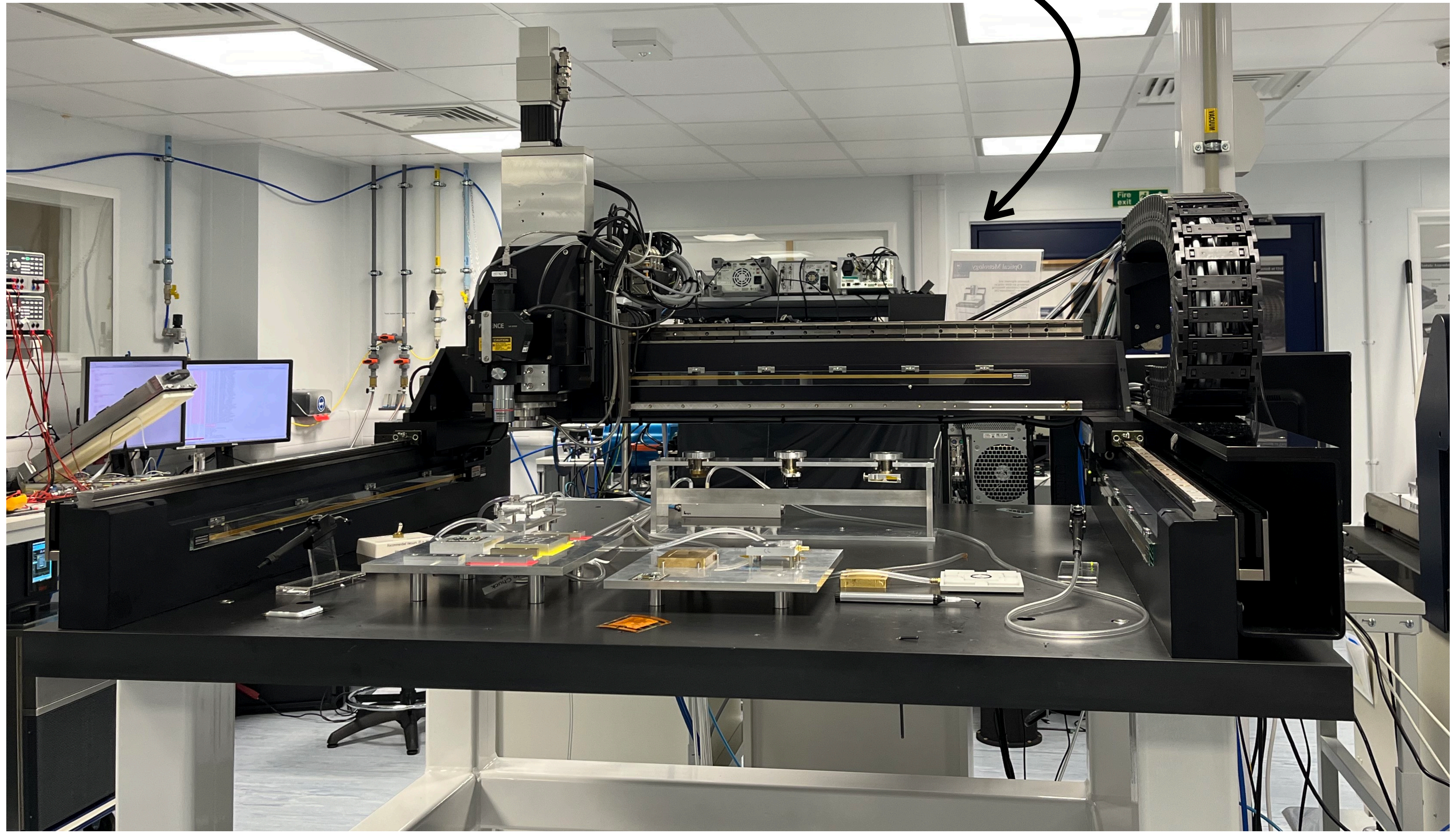
Significantly more, and larger, ladders required for outer pixels versus inner system. Exact ladder yield not yet known.

- **Total = 912 chips (central) + 2x912 chips (re-curl) versus 96 for vertex layers**
- Anticipate $\mathcal{O}$(60%) yield for pixel chips passing QC, further $\mathcal{O}$(60%) for ladder QC.
  - **Need to test 3x2000 chips in total!**

Production taking place @ Oxford

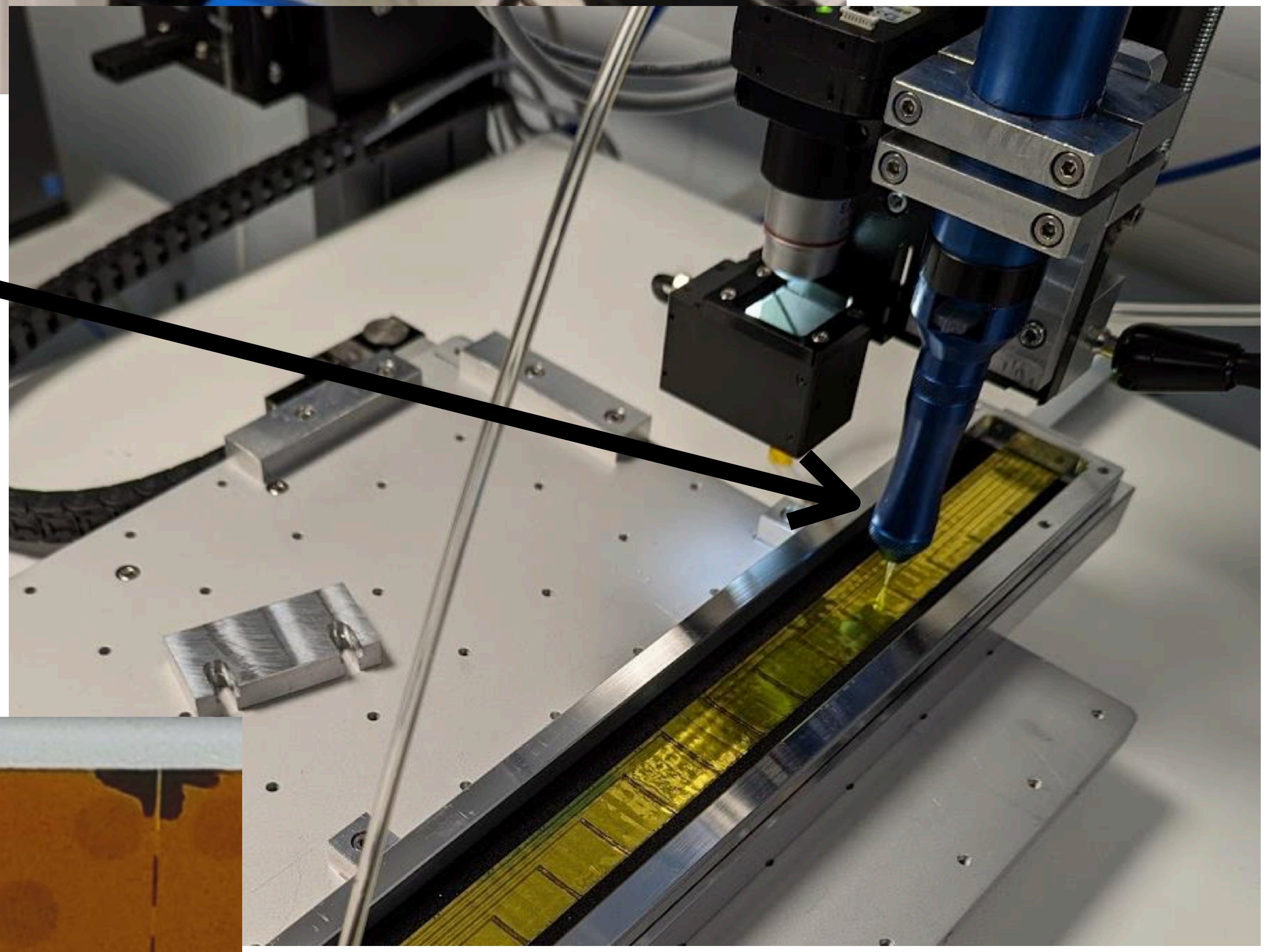
Automise ladder building procedure as much as possible:

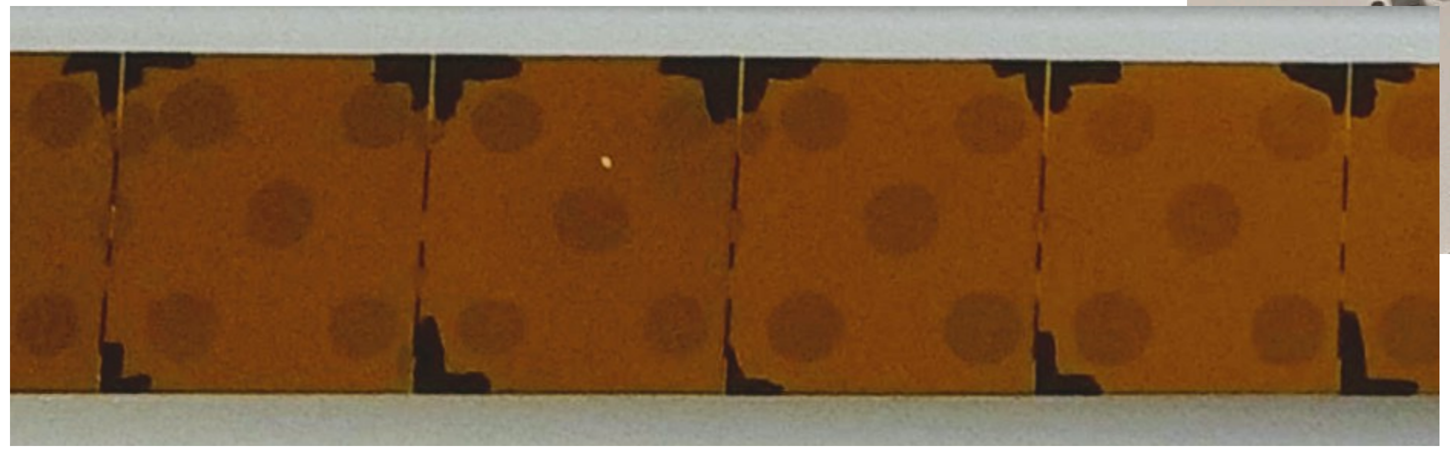
- Robotic gantry used for placement of chips on vacuumed ladder tool



Glue-dispensing robot

- Allows for precise placement (15 µm) and size of glue deposits





Outer pixel layer production status:

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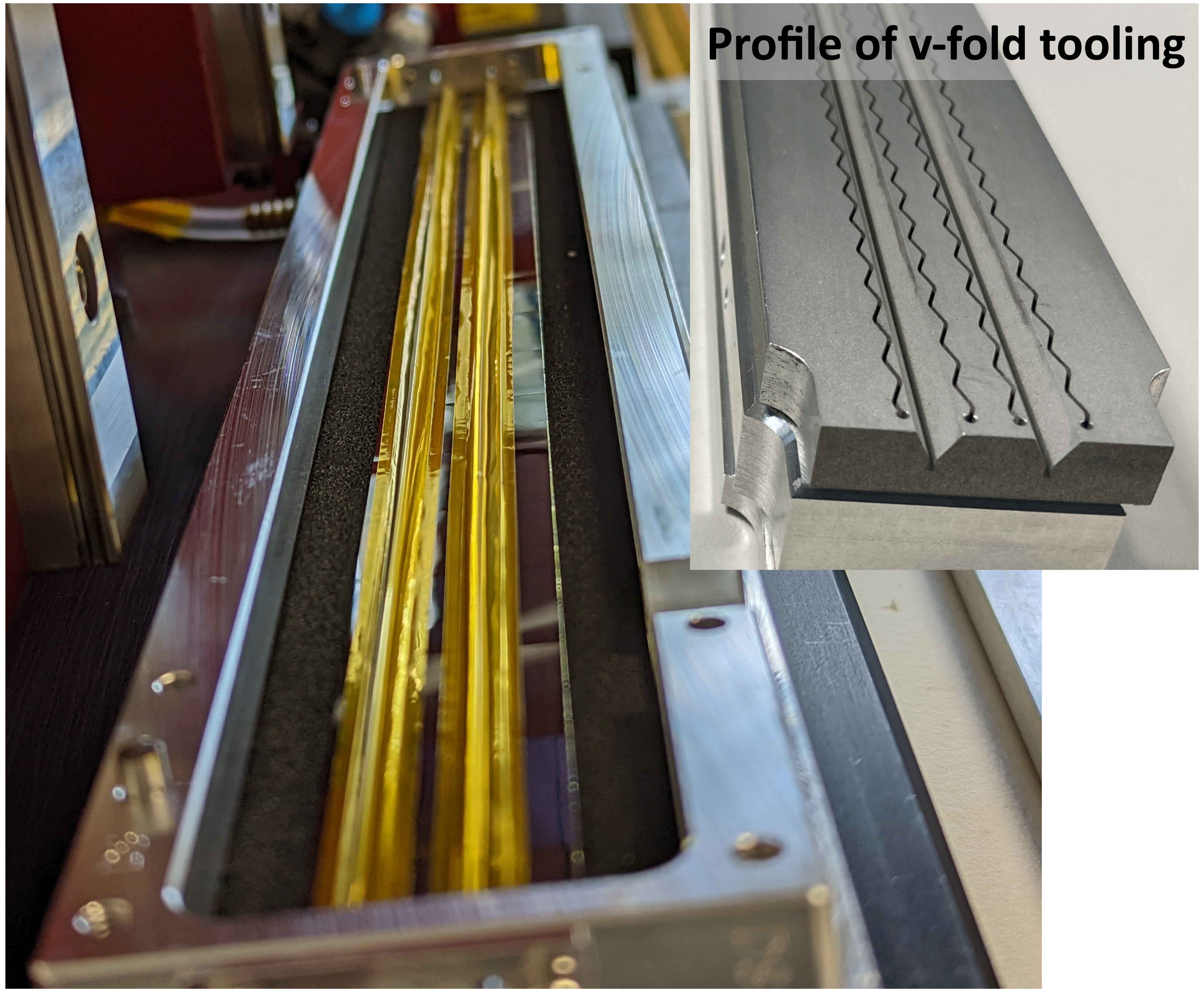
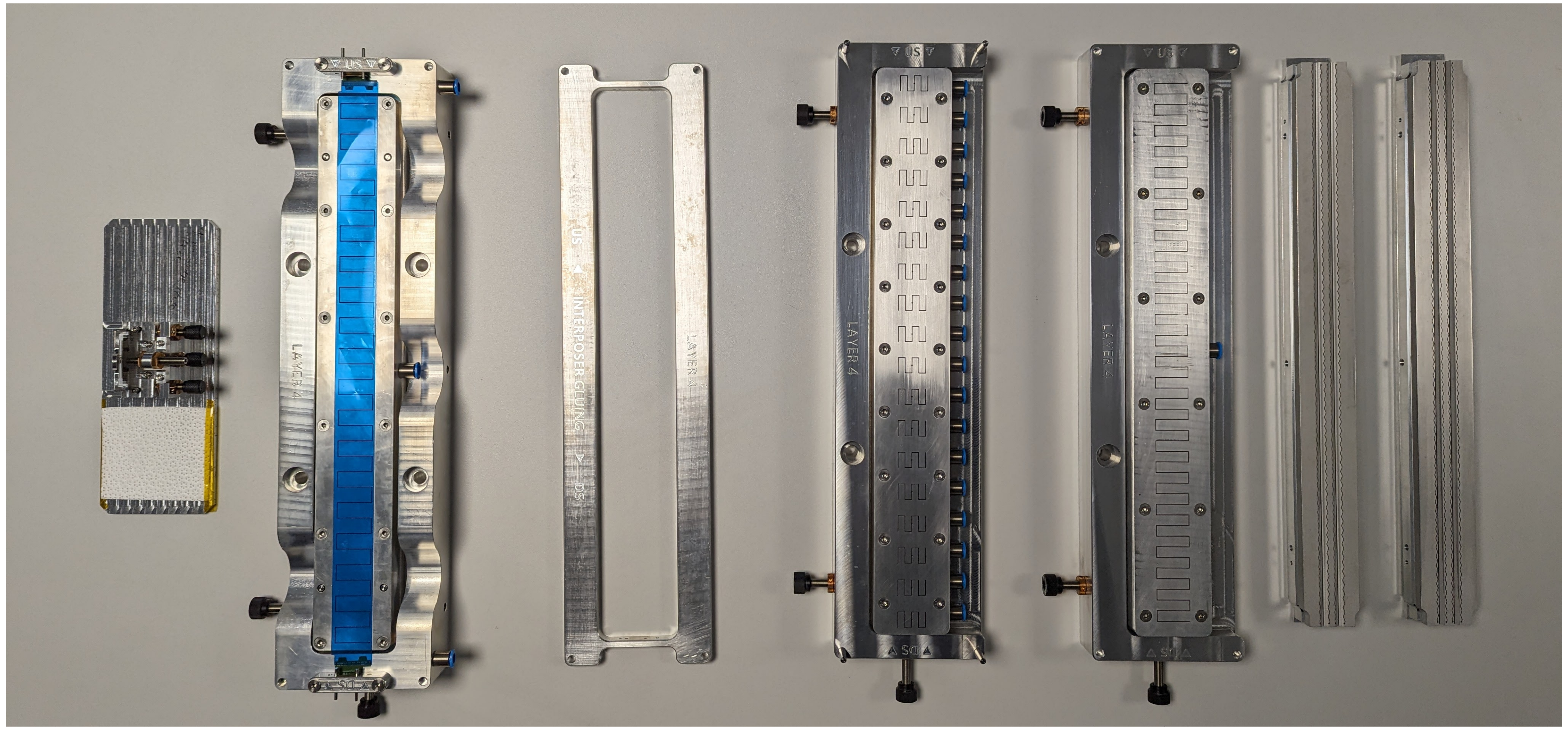
Production tooling for Layer 4 is almost complete, tooling for Layer 3 to commence shortly after.

- Expected production rate is $\mathcal{O}$(1.5 ladders / day), to commence March 2024

Prototype outer pixel layers have been fabricated.





Interposer flex bending tool	Align, glue, TAB bond interposer and ladder flexes	Ring frame to hold ladder during production	Chip chuck: align MuPix 11 array on robot and glue chips to ladder	Flex chuck for MuPix11 TAB binding, and V-fold gluing	V-fold and U-fold chucks

Mechanical stiffness of local support structure:

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V-folds initially proposed to be made from **kapton**

- **Difficult to fabricate**: **very flimsy** so if glue does not cover all edges sufficiently, risk peeling off ladder
  - Transportation issues?
- Enough structural integrity for 18 chip ladders, but not more (important for the future)

Alternate proposal: make **carbon-fibre u-folds**

- **Slightly lower mass than kapton**
- **U-folds**: rounded edge v-folds
  - Larger radius bend in carbon-fibre gives them greater mechanical stiffness
- Much easier to manufacture and handle (transport)
- Potential concerns about electrical cross-talk

Carbon-fibre ladder

Can hold 3 coins!

Kapton ladder

Visibly sags under it's own weight

Each object with steel chips weighs $\sim$ 5g, corresponding to $\approx$ 2 grams for Si chips!

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Carbon-fibre ladders:

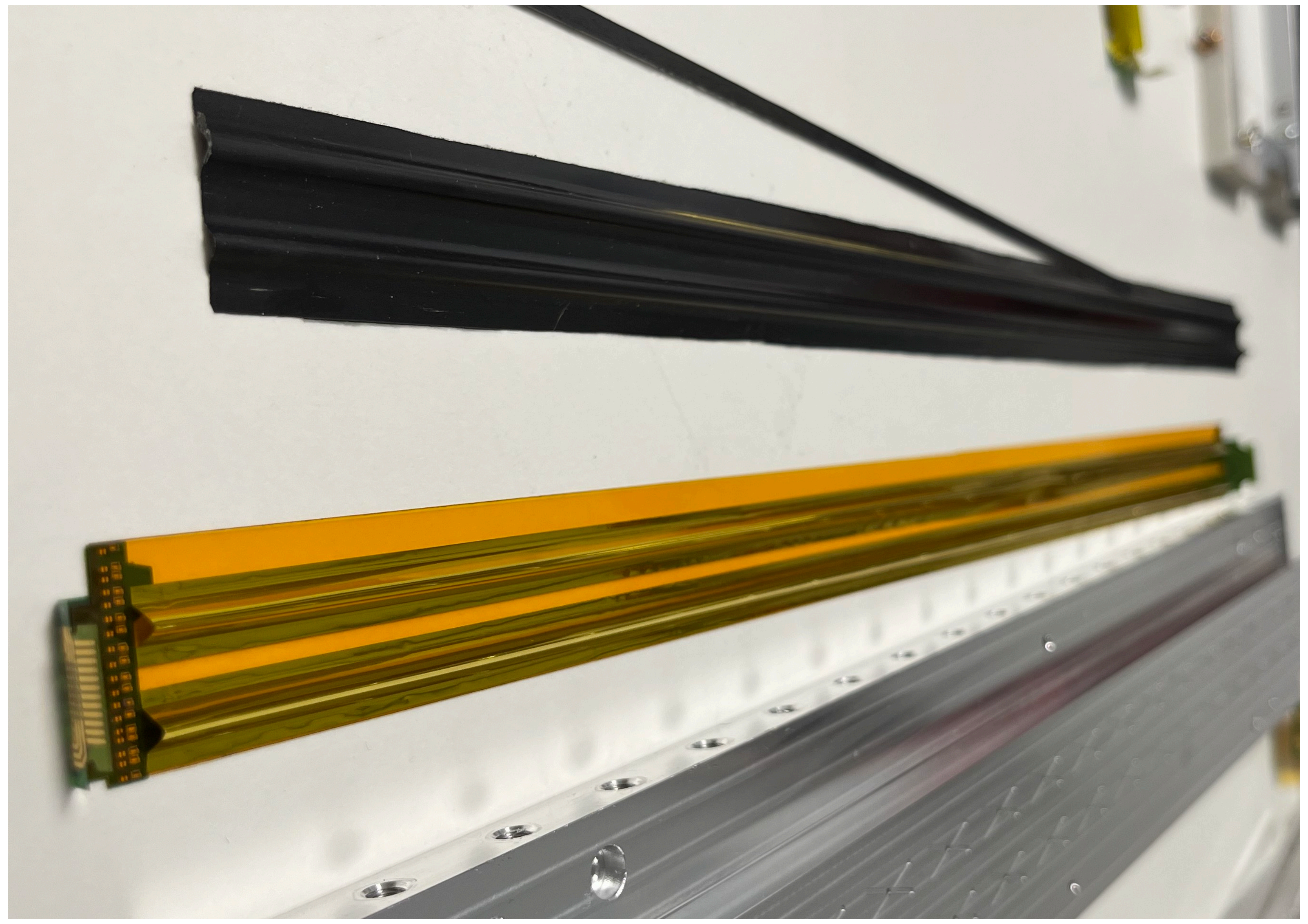
Test ladders made so far from 60μm thick uni-directional carbon-fibre, with joined u-folds:

- ATLAS pre-preg: Mitsubishi K13C2U and Cyanate Ester EX1515 matrix

Future:

- 30μm also available: tow spread Tairyfil TC33 fibre and SK Chemicals K51 matrix
- Ultimately **15μm thickness**: via informal contacts with Renault F1 thanks to our engineering team

- Likely combine with thin kapton backing (to ensure no electrical contact between ladder halves)



Construction on-going for **test ladder objects of both kapton and carbon-fibre**

- Production of carbon-fibre prototype ladders in progress: strong collaboration with mechanical workshop @ Oxford
- Perform mechanical and electrical tests on both

Results from thermal cycling ladder prototypes:

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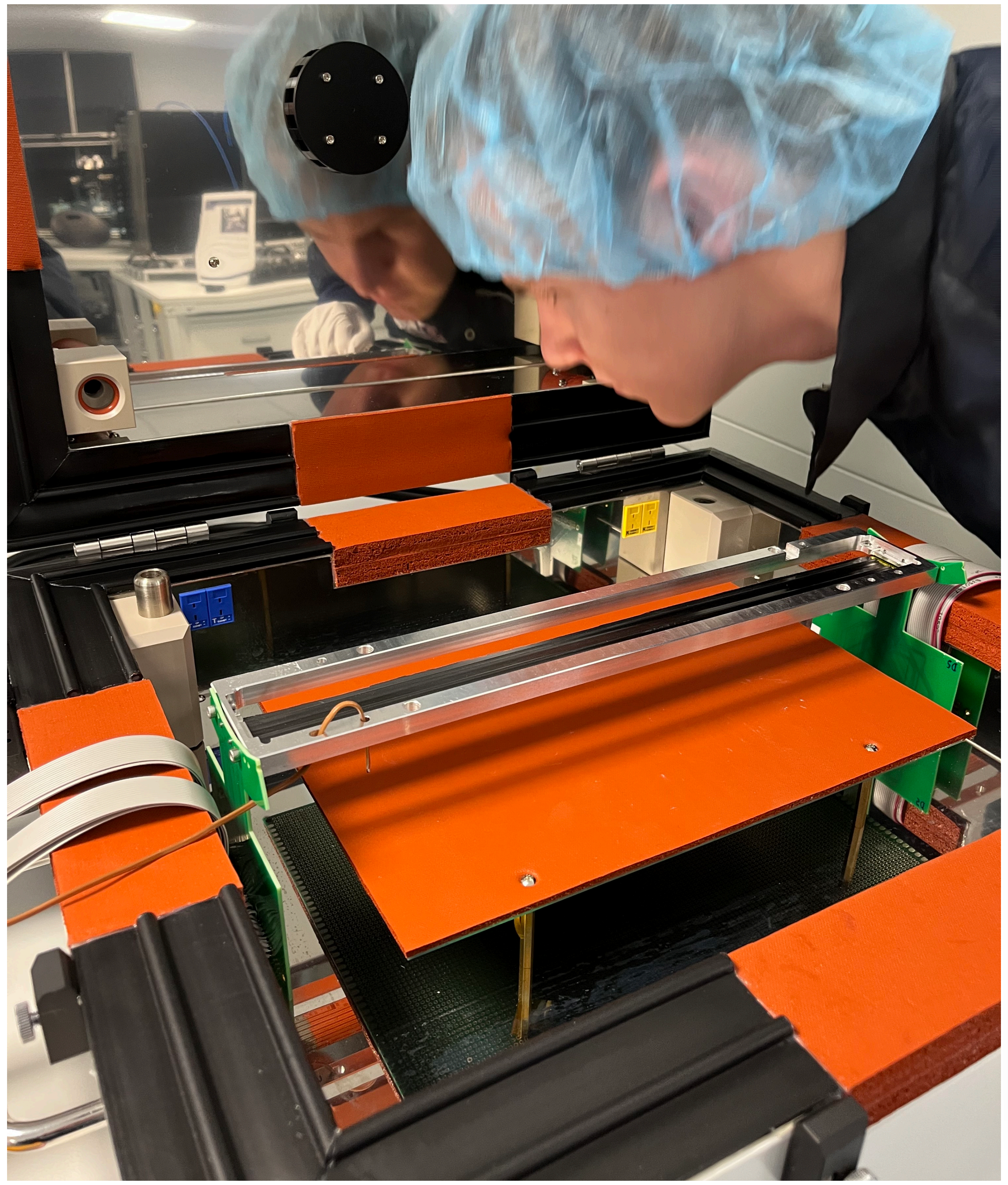
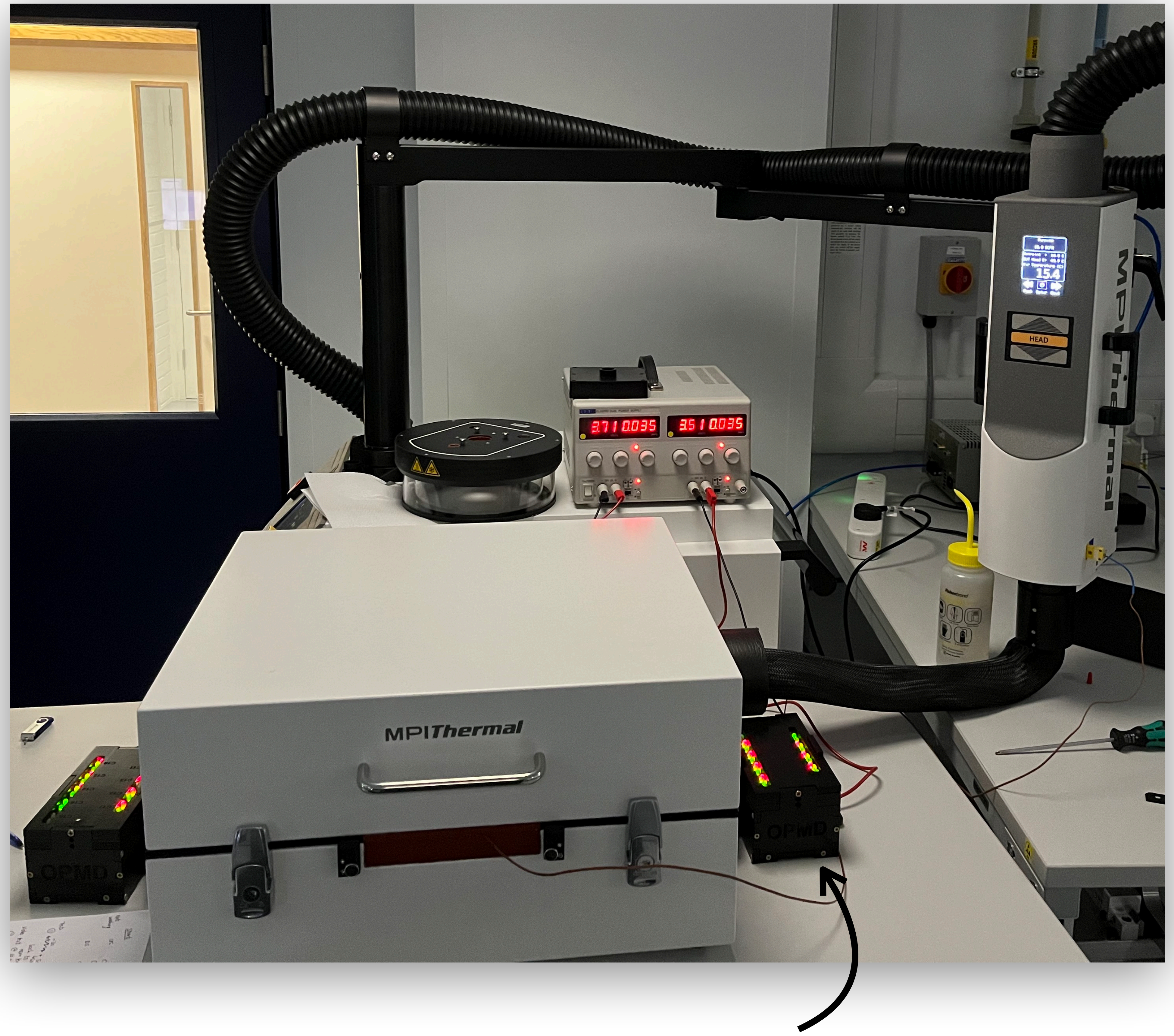
First test of **electrical connectivity**: using ladders made with silicon heaters

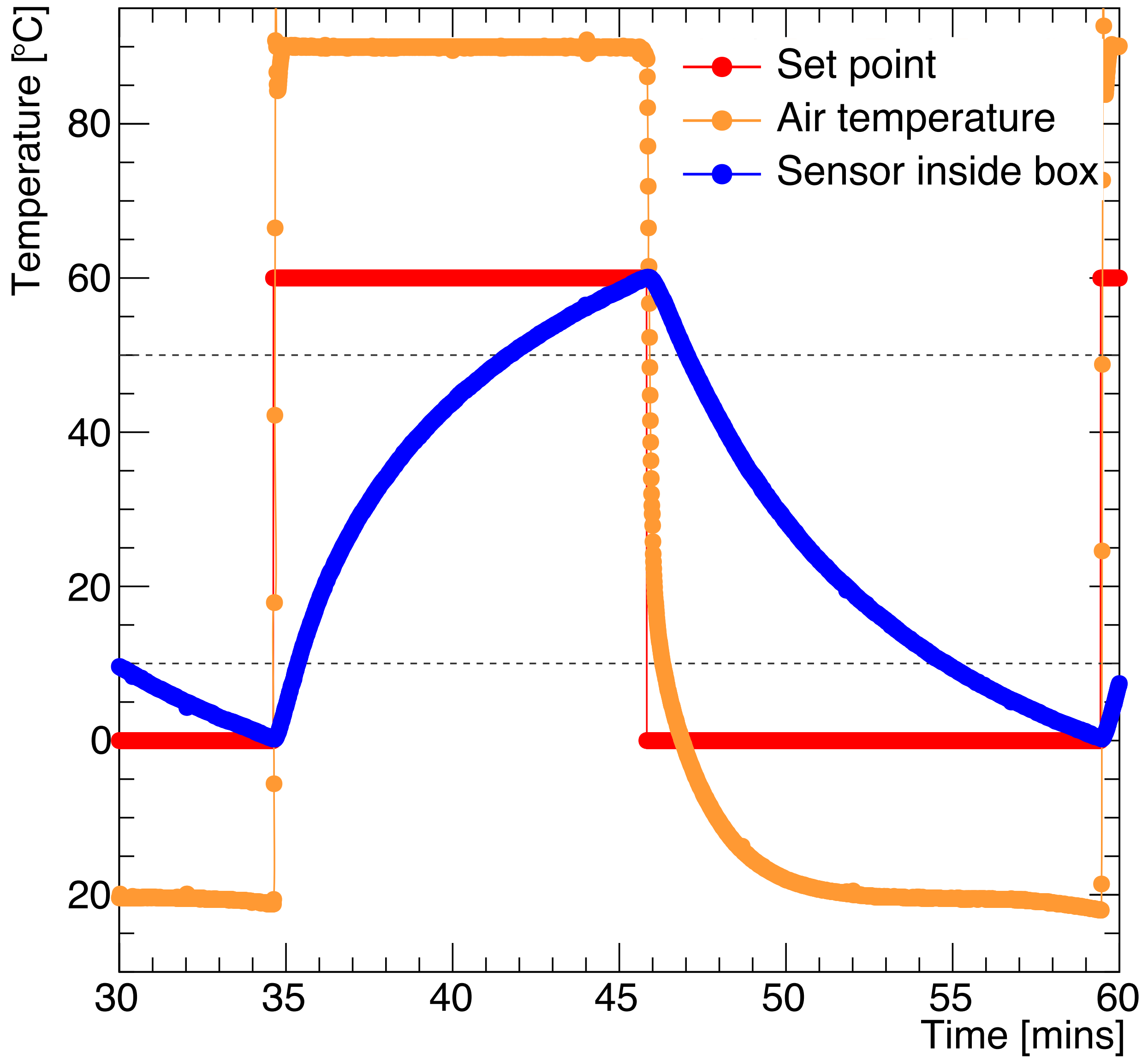
- LEDs soldered to monitor in real-time the connectivity of the 4 sense (green) + power (red) lines per chip
- Thermal cycle between expected operational temperature range ($0 \rightarrow 60$°C) to check for failures



Thermally insulated box



Thermal cycling system, LEDs remain outside



50 cycles completed:

- 2 failures seen (initially poor connections)

Now extended ΔT = $-20 \rightarrow 60$°C

- Same test for kapton v-fold ladder in progress

Quality control for silicon pixel chips:

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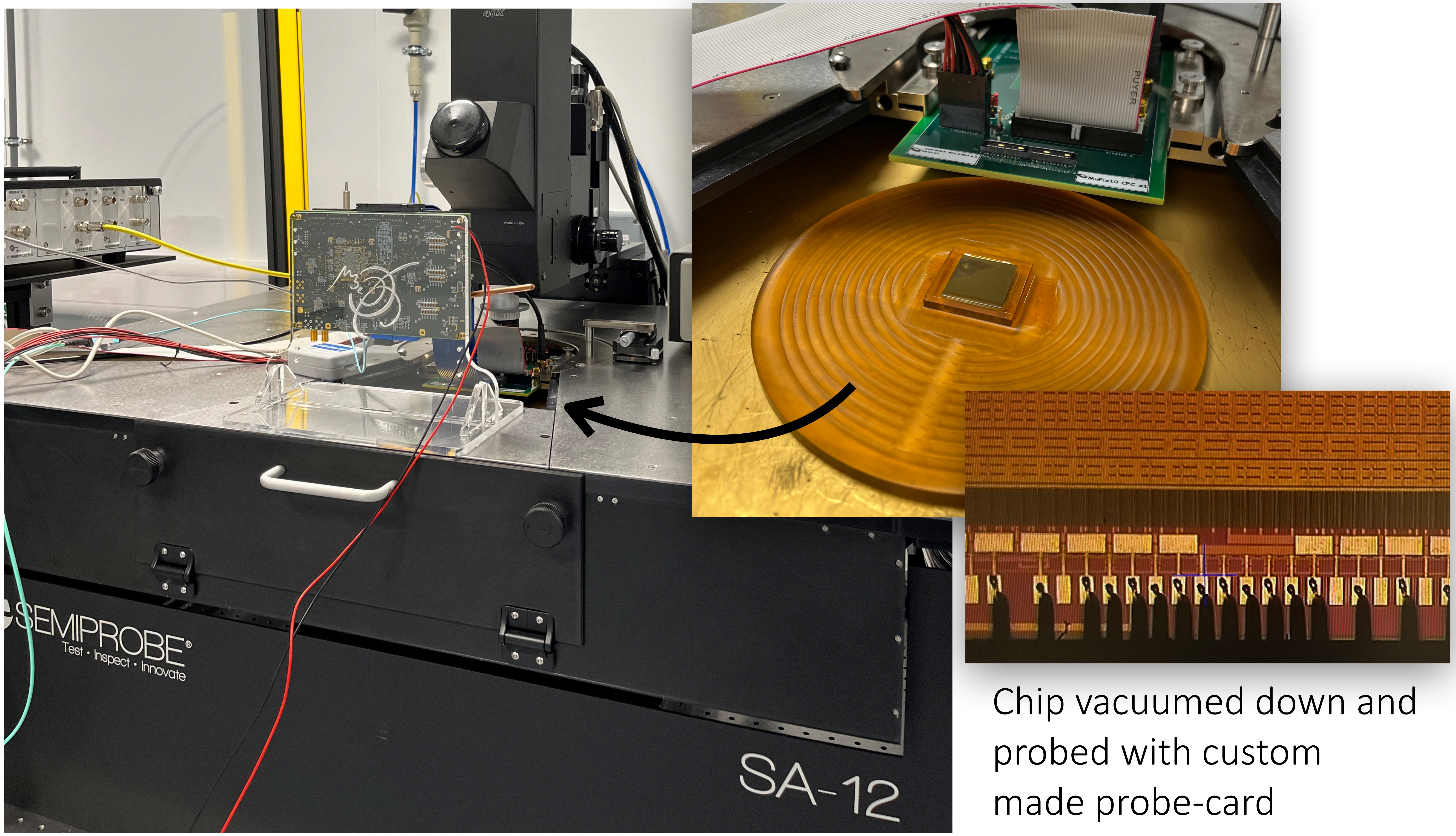
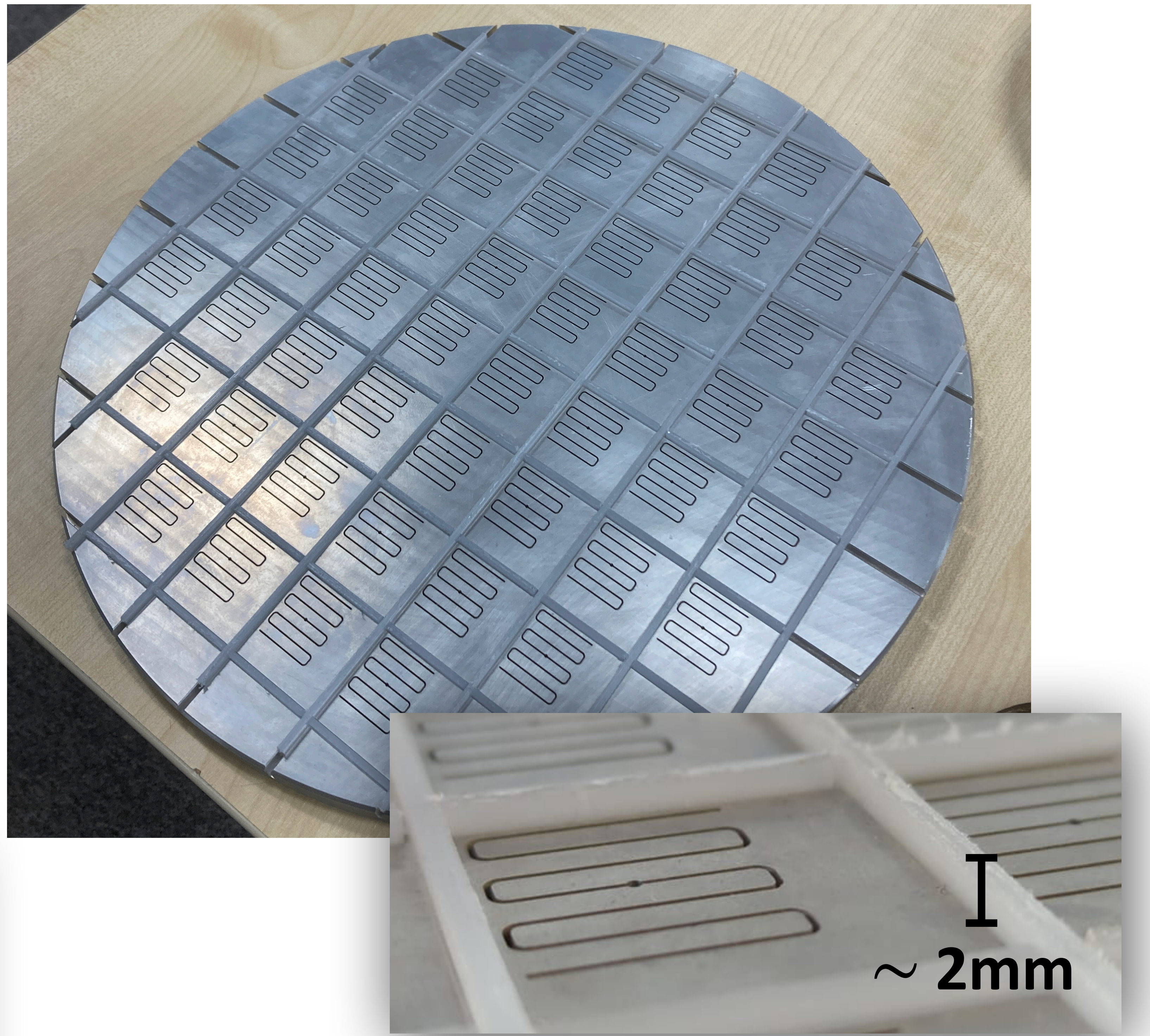
Use semi-automatic probe station @ Oxford to conduct QC tests on all pixel chips required for construction of outer pixel system.

Single-chip testing: establish QC procedure



Chip vacuumed down and probed with custom made probe-card

Wafer testing: required for ladder production



- Chips held with vacuum individually
- Raised edges allow for chip alignment
- Use pattern recognition to identify individual chips and low to pre-set height to make needle contact
  - Conduct QC tests

Coming soon:

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Mu3e: search for cLFV - aiming to measure the BR($\mu \rightarrow eee$) with unprecedented sensitivity!

- Ultra light-weight detector using custom designed HV-MAPS pixel sensors (MuPix11) for the inner and outer pixel layers, to detect electrons and positrons
- MuPix chip development at the forefront of HV-CMOS R&D

Detector construction in progress:

- Expected full Mu3e detector integration + commissioning to take place mid 2024

Expected to start taking physics data in 2025 (Phase I):

- Beam available until ~ end 2026 —> shutdown (—> Phase II)
- Plans to upgrade existing muon beam to increase intensity
- High intensity muon beam (HiMB) project is under discussion
  - Would provide muon intensities $> 10^9$ μ /s
  - Ultimate experimental sensitivity limited by this rate

Stay tuned … !

[Mu3e collaboration] | [Oxford silicon detector group] | [ashley.mcdougall@physics.ox.ac.uk]