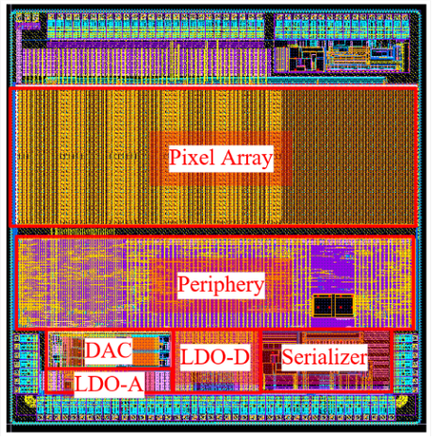
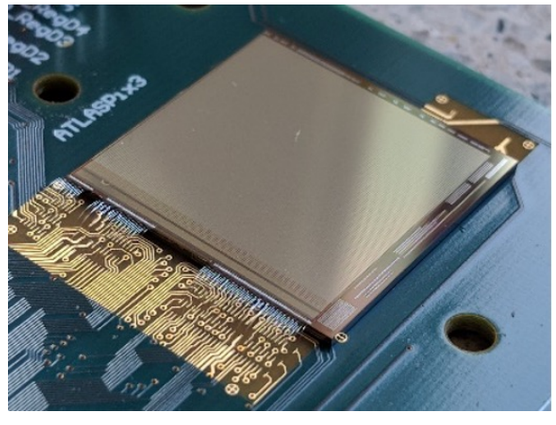


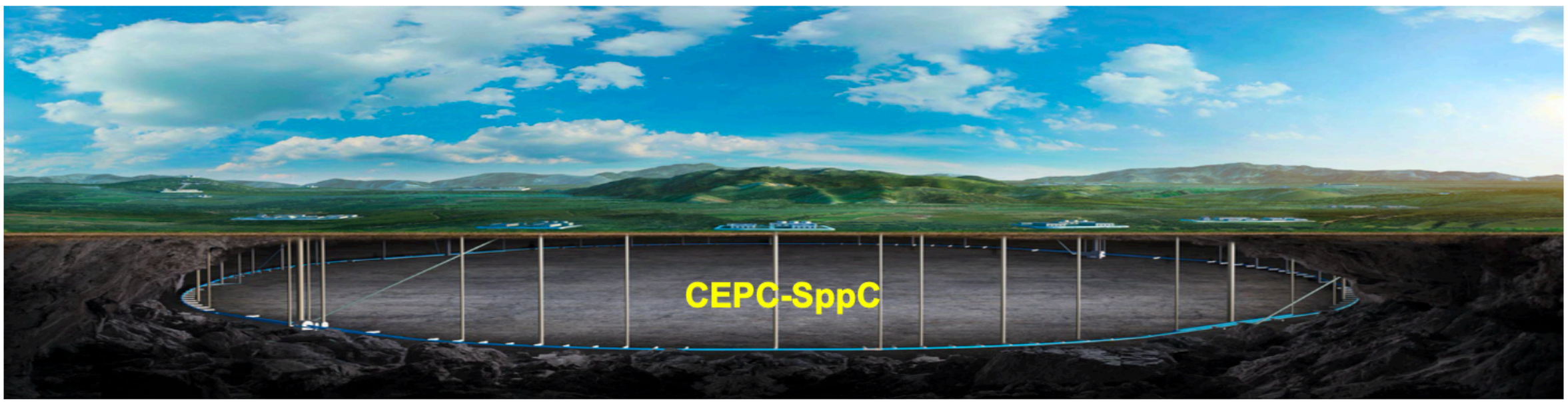


Summary of vertex and tracker developments at CEPC

Yanyan Gao (University of Edinburgh)

Current and future vertexing and tracking detector 2023

QMUL 7-November-2023

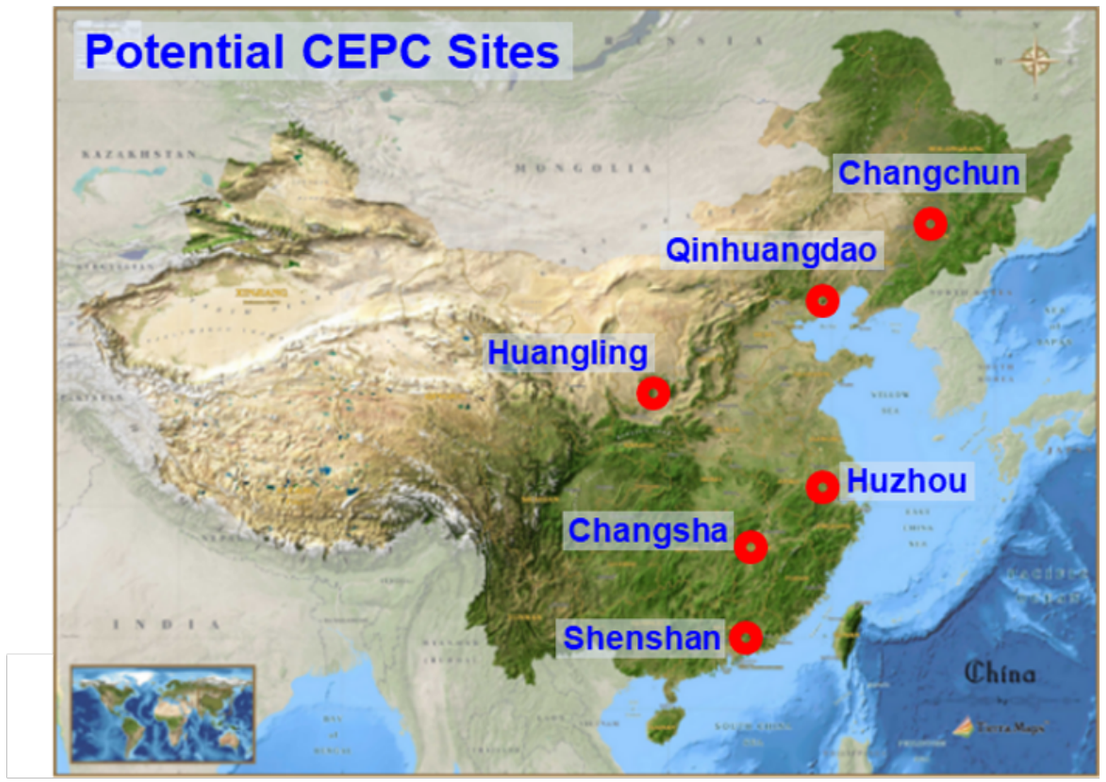


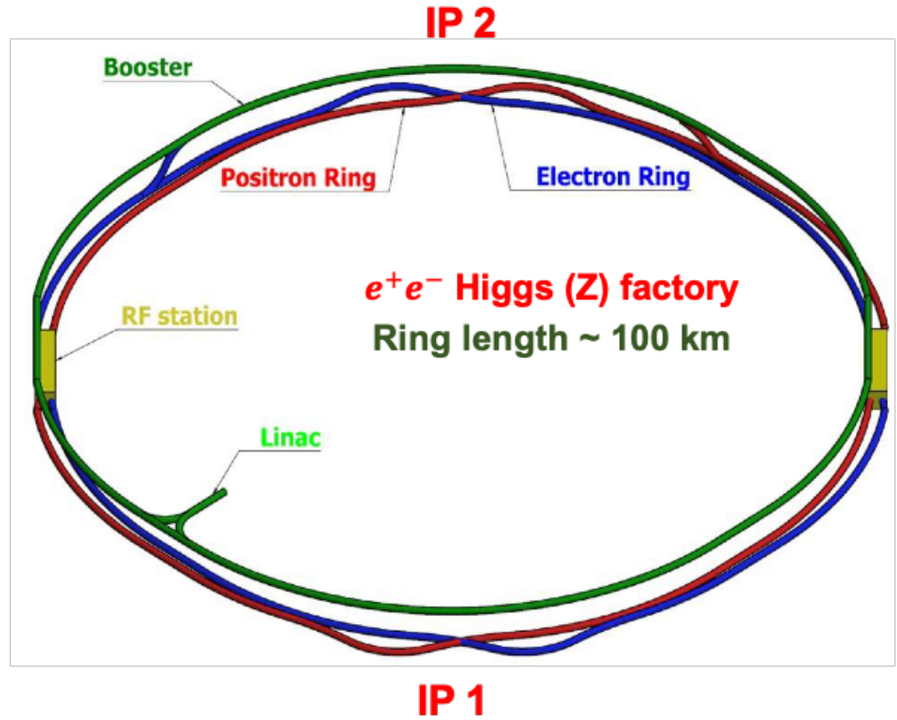
Overview

- This talk focuses on the silicon-based R&D effort in the CEPC community
  - Not covered: gaseous detectors, SOI technology, large area stitching
- Vertex detector R&D
  - Funded and led by China, covering many key areas from sensor to system prototyping
- Tracker R&D
  - Large international effort on system design based on existing ATLASPix3 sensors
  - KIT is leading future sensor improvements with TSI 180nm and 55nm foundries in China
  - China-led LGAD R&D for Time-Of-Flight detector (synergy with ATLAS HGTD effort)
- Most material is based on CEPC detector CDR and the latest CEPC workshops in 2023
  - Nanjing Workshop Oct 2023: https://indico.ihep.ac.cn/event/19316/
  - Edinburgh Workshop July 2023: https://indico.ph.ed.ac.uk/e/cepceu2023

The CEPC Higgs factory proposal

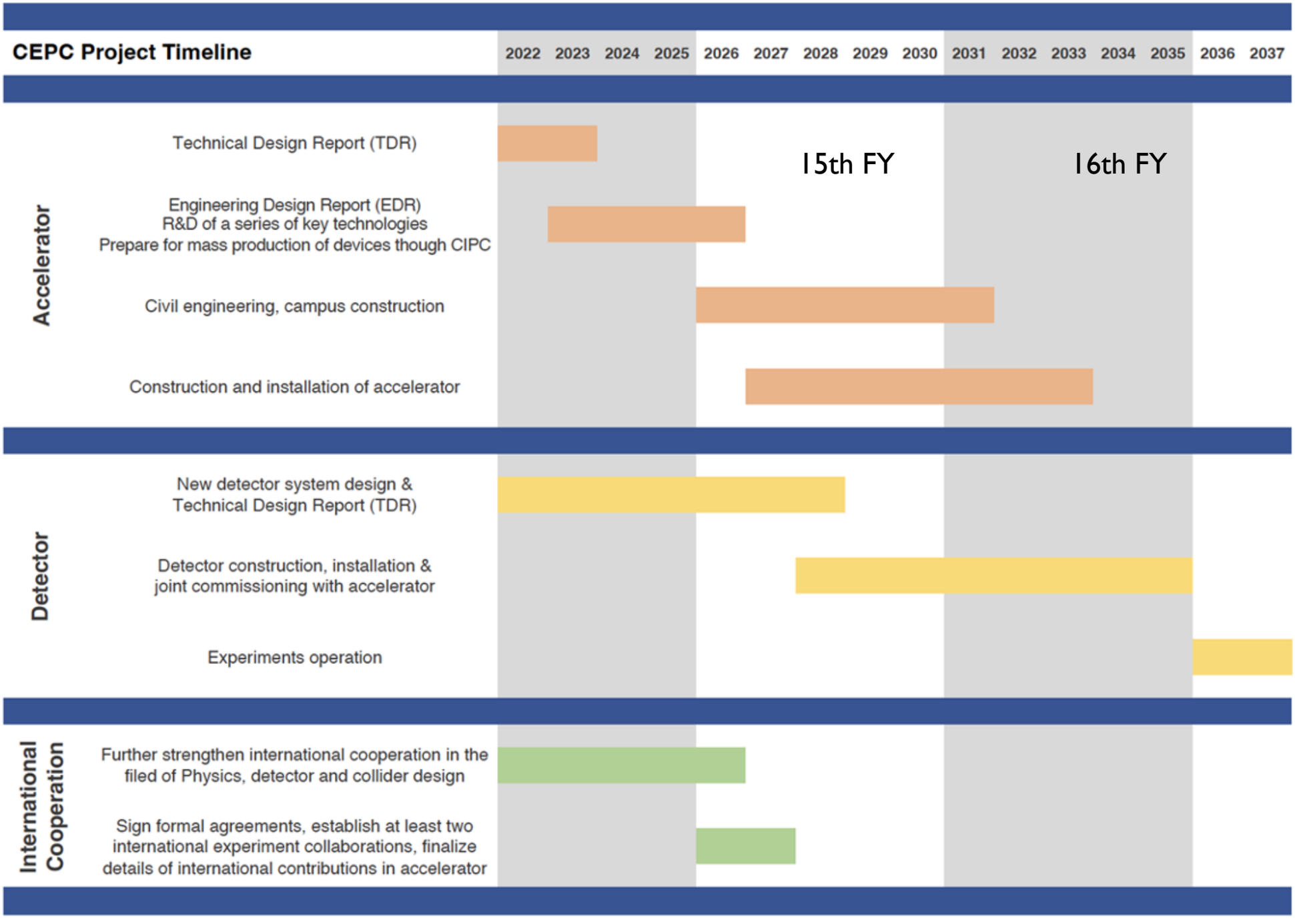
- The CEPC, 100-km e+e circular collider was proposed in 2012 as a Higgs factory by China
  - big international project
  - pre-CDR released in 2015
  - Accelerator and detector CDR released in 2018
  - Accelerator TDR has completed after international review and to be released in Nov 23
    - Next milestone is EDR (2026)
  - Detector TDR is being discussed for 2024-25
- Latest operation plan includes
  - 10 years Higgs, 2 years Z, 1 year WW, 5 years ttbar
  - Luminosity and rates at Z-pole running poses the most stringent requirement on detector
- pp collider (SppC) of 50–100 TeV after CEPC





CEPC timeline

- Construction starts as early as 2027-28 for operation ~2035 in the middle of HL-LHC
  - Key considerations in detector technology R&D: maturity and accessibility



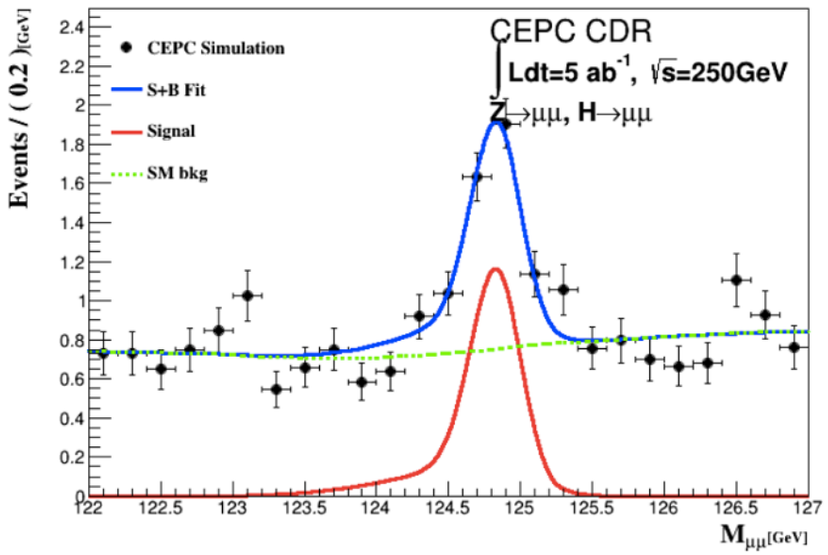
Link to Yuhui Li's talk in the 2023 CEPC Nanjing workshop

Physics motivation - key processes

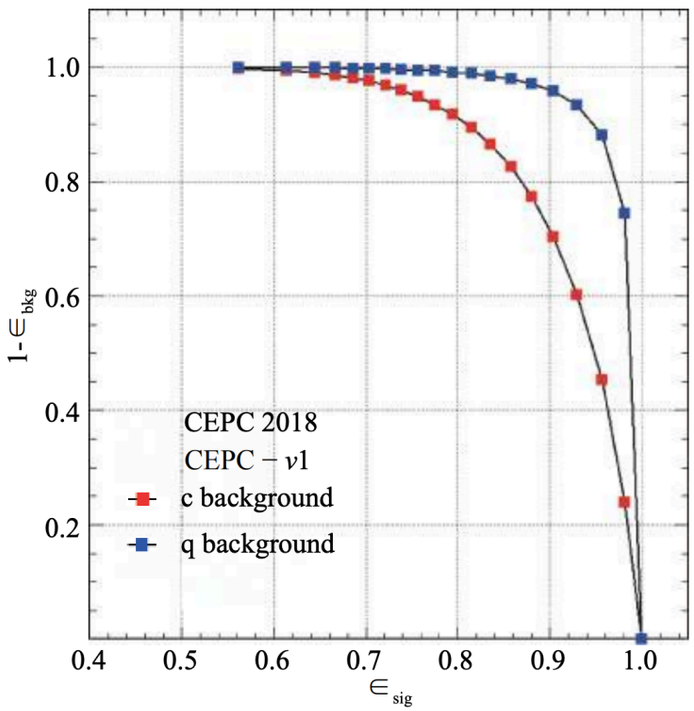
Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV})\sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} =$ $5 \oplus \frac{10}{p(\mathrm{GeV})\times\sin^{3/2}\theta}(\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	$\mathrm{BR}(H \to q\bar{q}, WW^*, ZZ^*)$	ECAL HCAL	$\sigma_E^{\mathrm{jet}}/E =$ $3 \sim 4\%$ at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\Delta E/E =$ $\frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$

Overall aim for up-to an order of improvement compared with the LHC experiments

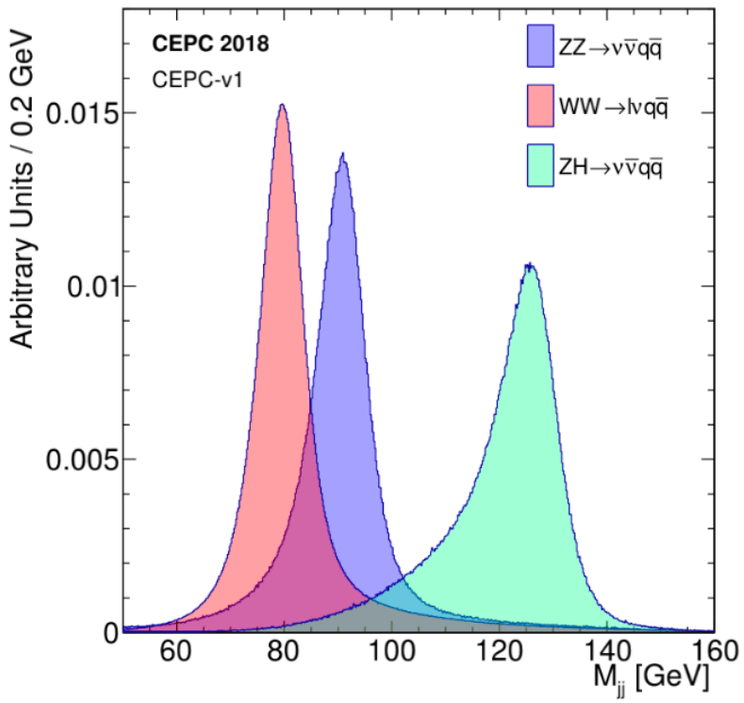
Particle level PID



Track momentum resolution



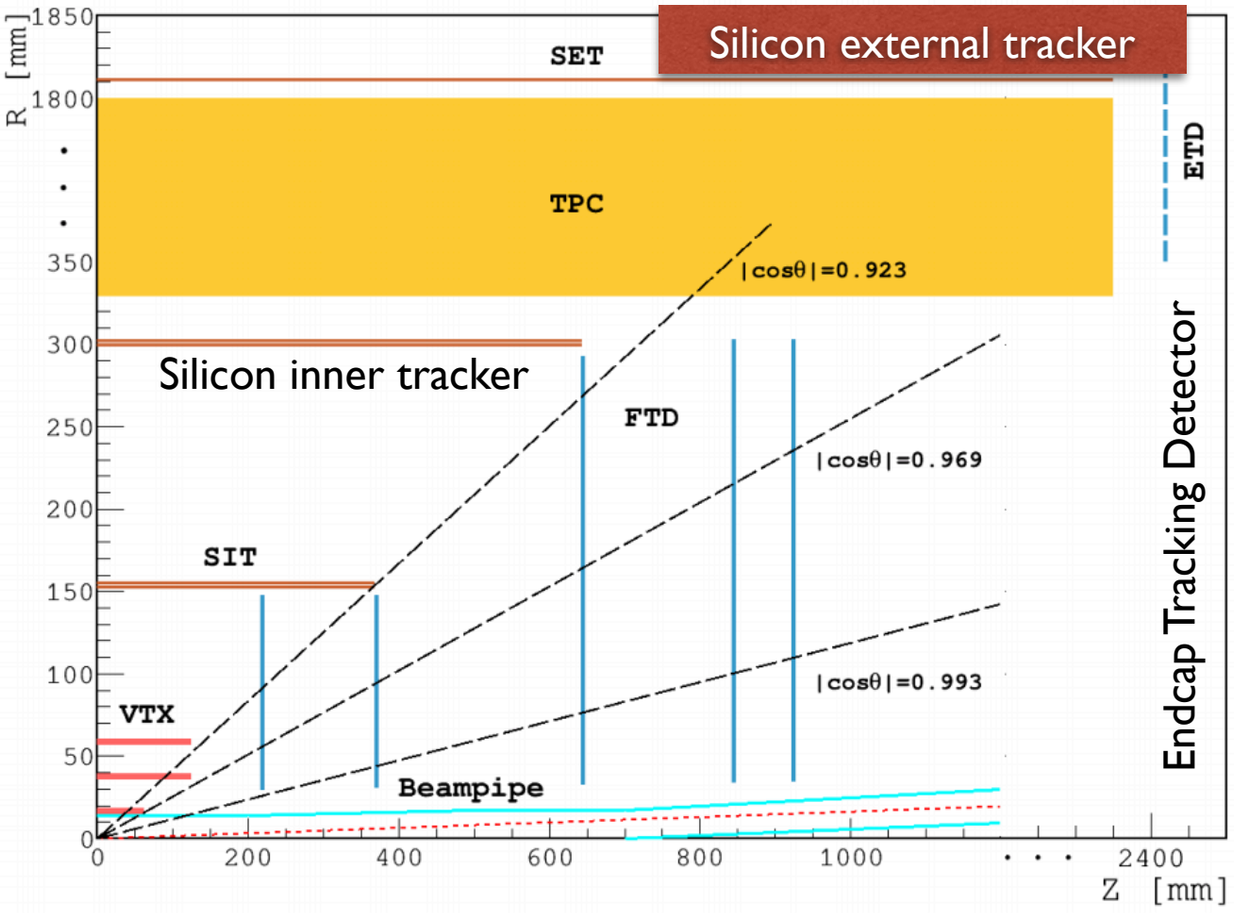
Heavy flavour tagging



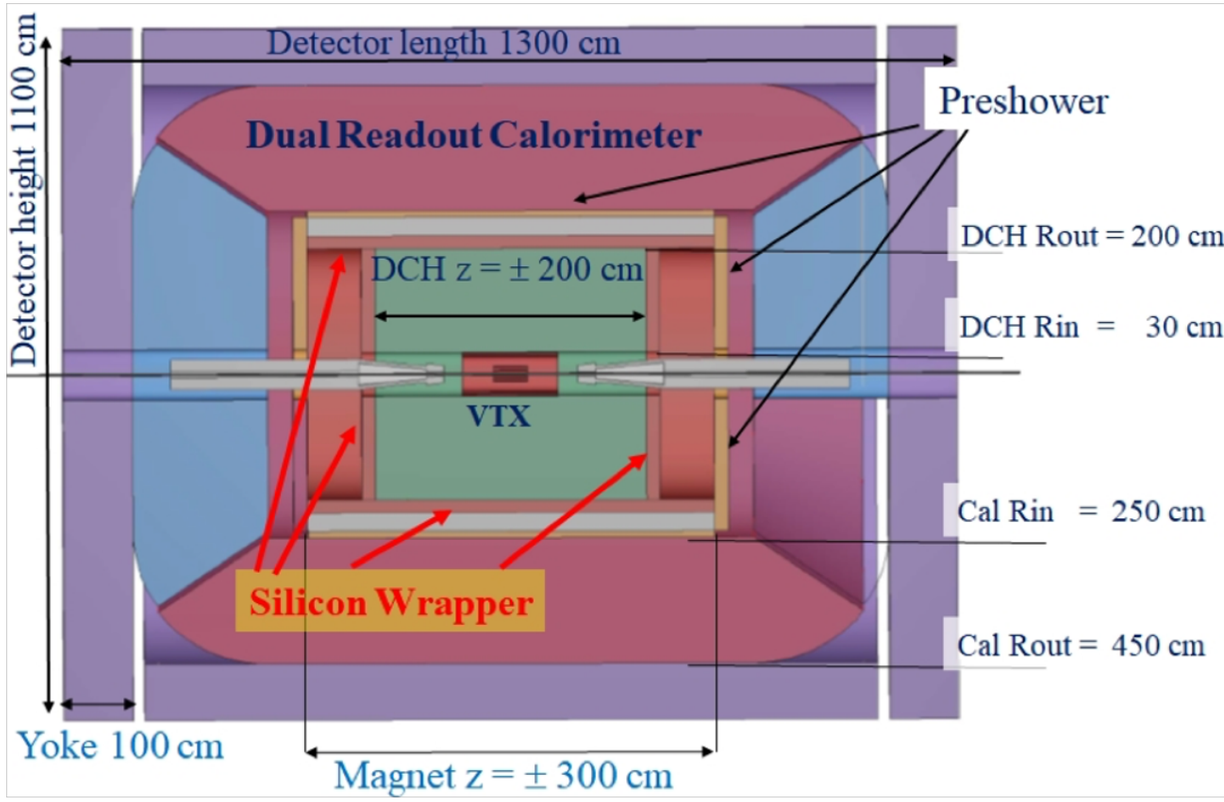
Jet energy scale (PFA)
W/Z hadronic separation

CEPC detector concepts

- Four detector concepts have been studied, all requiring precise vertexing and tracking
  - Vertexing: depleted MAPS is considered as the technology of choice (SoI is also investigated)
  - Central tracking: silicon (MAPS/strips/pixel-strip hybrid), TPC or DCH (2T)
  - Additional timing layer based LGAD for PID is also being considered



High B (3T) ILD-like concept - particle flow approach



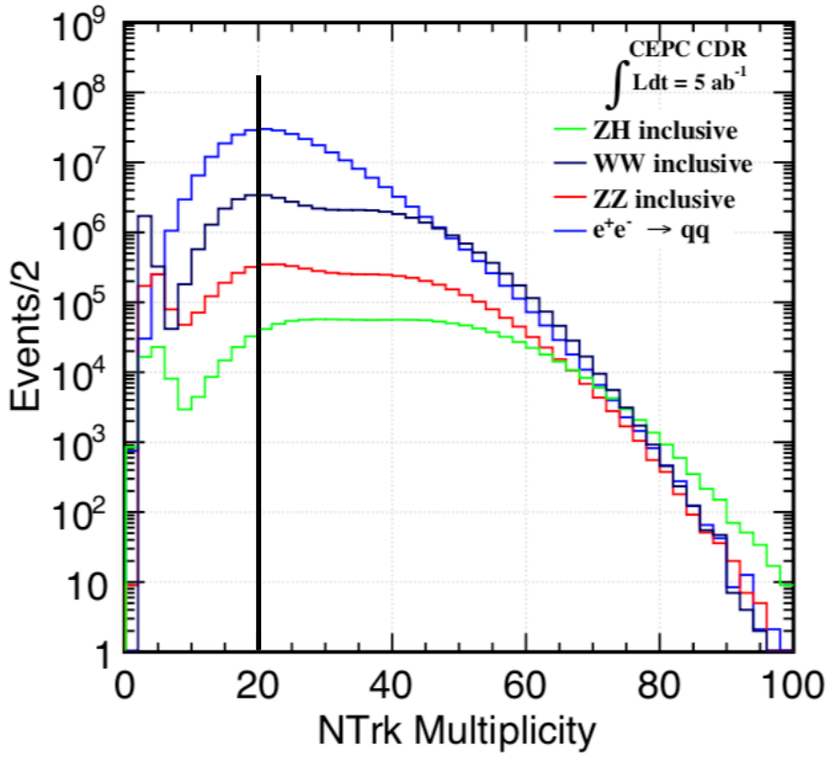
Low B (2T) IDEA concept

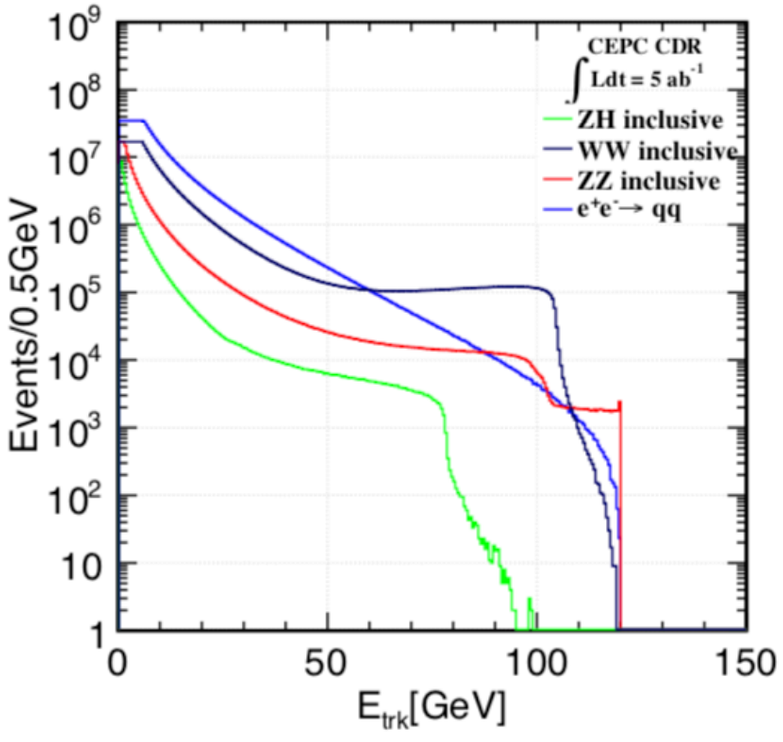
Tracking environment

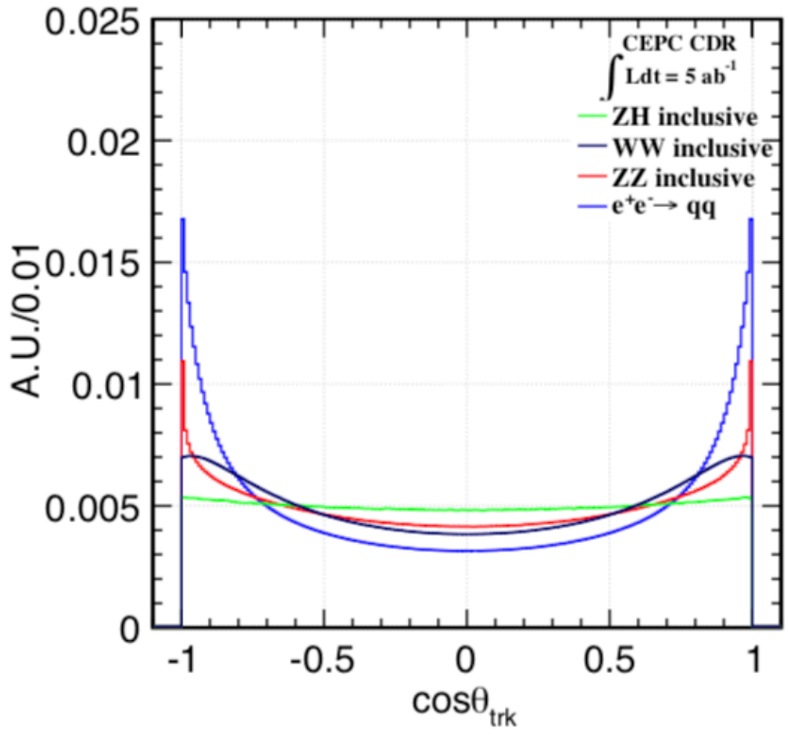
- For CEPC, particles are typically << 50 GeV multiple scattering has a significant impact

Higgs running @ 240 GeV

pT > 0.5 GeV



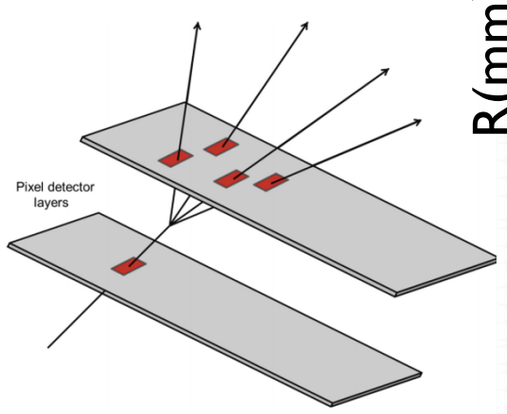


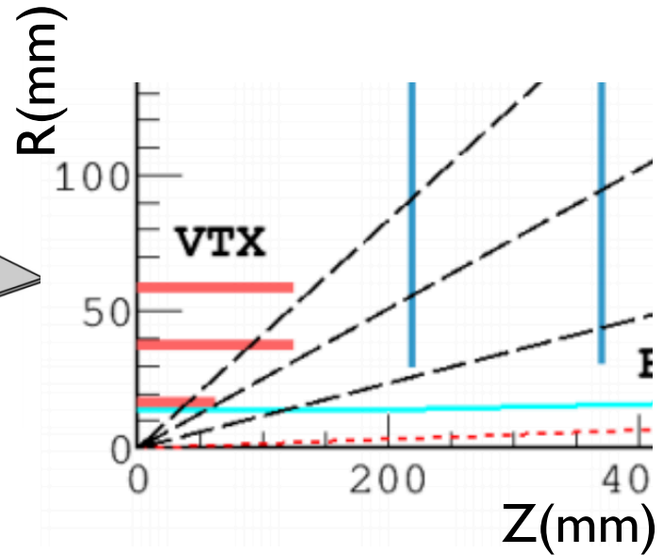


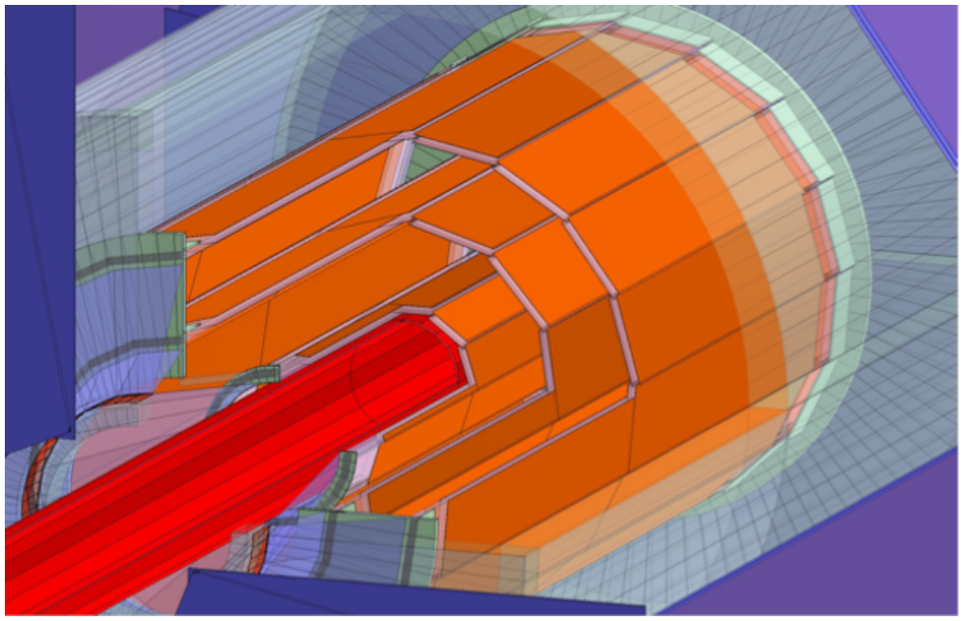
For the Z-pole running, track pT < 45 GeV, except a bit lower multiplicity

Vertex detector - key requirements

- Small inner radius, close to beam pipe
  - new baseline beam pipe R=10mm
- Design priorities
  - High spatial resolution near the IP (3-5 um)
    - High granularity, small pixel pitch
  - Low material budget <0.15% X_0 per layer
    - Very thin sensor, air cooling, power disp. < 50mW/cm^2
  - Global time resolution of CEPC tracker: ~25ns (40MHz collision @ Z pole)
  - Inner most layer (16mm) @ Higgs running
    - Hit density ~2.5 hits /cm^2 / BX
    - 2.5 MRad/year (TID) and 10^{12} neq/cm^2 (NIEL) with SF of 10 applied
- Technology of choice: pixel MAPS
  - 3D SOI: link to Yang Zhou's talk at the 2023 CEPC Edinburgh workshop

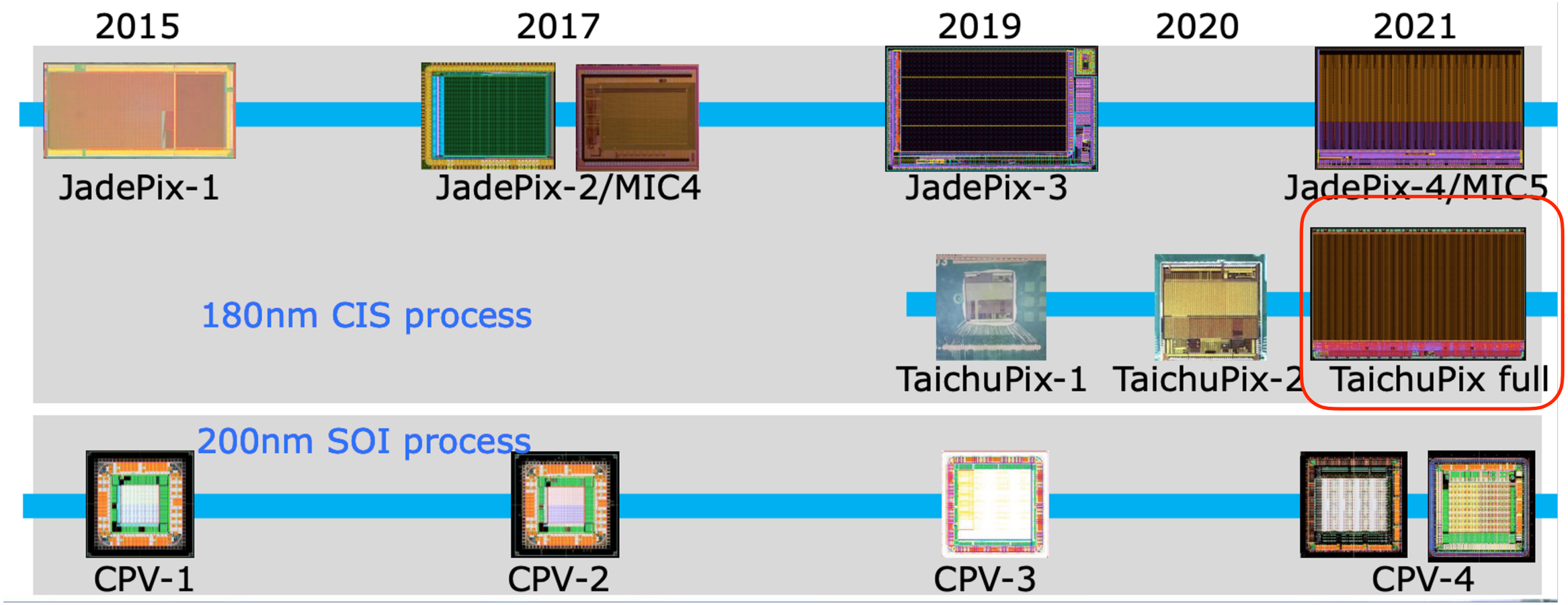






Roadmap of sensor R&D for vertex detector

- Vertex detector R&D has been flagged a critical area
  - Focus is on silicon CMOS sensor R&D, aiming for feasibility studies for the full chain
- Nearly a decade's effort that culminated in the full size TaichuPix3 ER in 2022



Link to Zhijun Liang's talk at the 2023 CEPC Nanjing workshop

Research funding and team

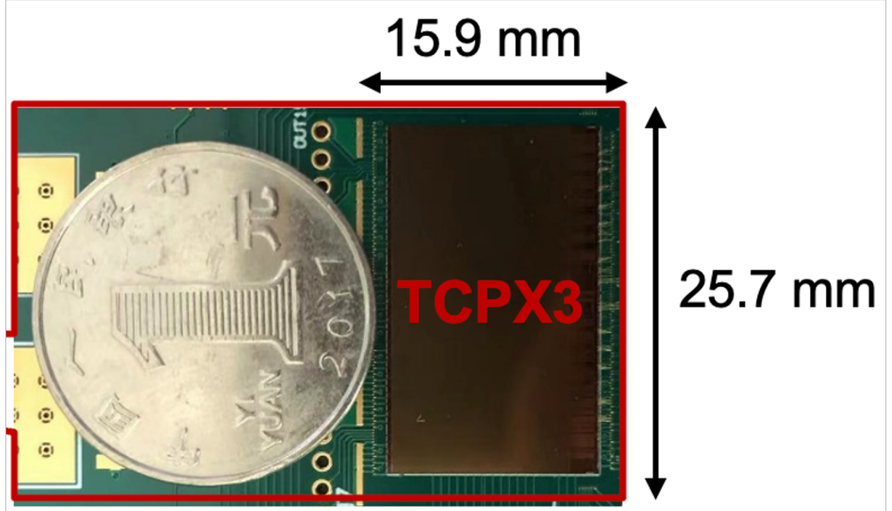
- Ministry of Science and Technology (MOST) funded two CEPC projects from 2016-2023
  - Vertex detector received ~£1M (2016-2021) and £1.5M (2018-2023), excluding staff time
- Impressive effort from China with limited international collaboration (esp. COVID19)
  - UK (Liverpool and Oxford) contributed to the MOST1 on mechanic design (no funding access)

Institutes	Tasks
IHEP	Full CMOS chip modeling, Pixel Analog, PLL block Detector module (ladder) prototyping Data acquisition system R & D Vertex detector assembly and commissioning Irradiation, test beam organization
IFAE(Spain)/CCNU	CMOS sensor chip: Pixel Digital
NWPU	CMOS sensor chip: Periphery Logic, LDO
ShanDong University	CMOS sensor chip: Bias generation, TCAD simulation Sensor test board design
Nanjing University	Irradiation, test beam

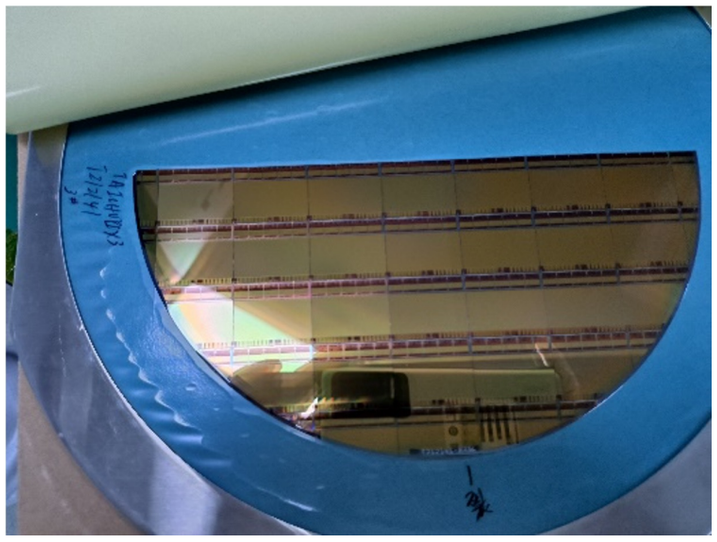
Link to Zhijun Liang's talk at the 2023 CEPC Nanjing workshop

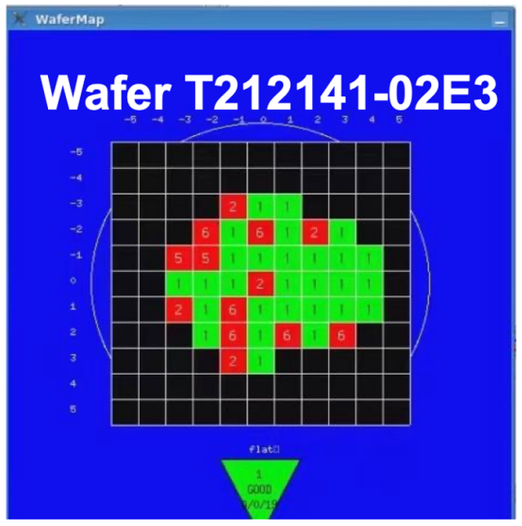
Fullsize TaichuPix3 prototyping (ER 2022)

- The first full-size CMOS pixel sensor for particle detector in China
  - Towerjazz 180nm CIS process
  - Chip Size 15.9×25.7mm
  - Pixel array: 1024×512
  - 25μm×25μm pixel size
  - Fast Periphery digital readout , high-speed data interface

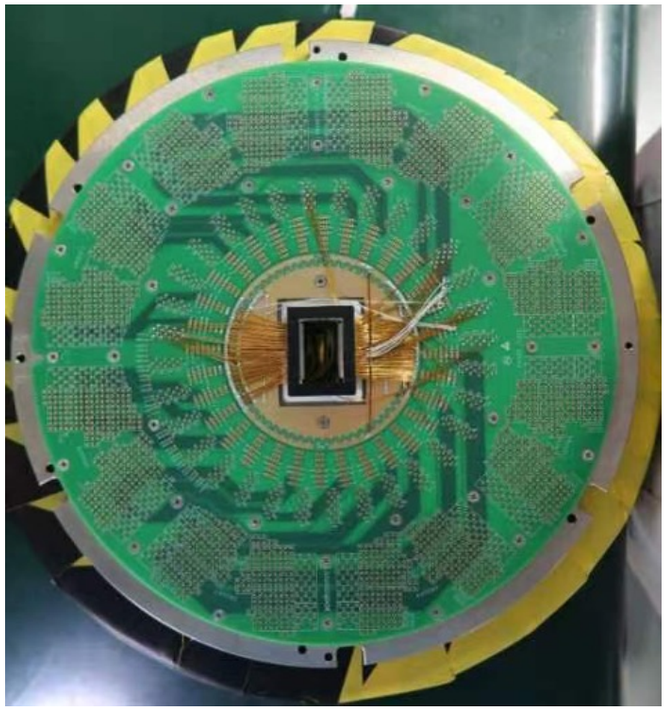


TaichuPix-3 chip vs. coin





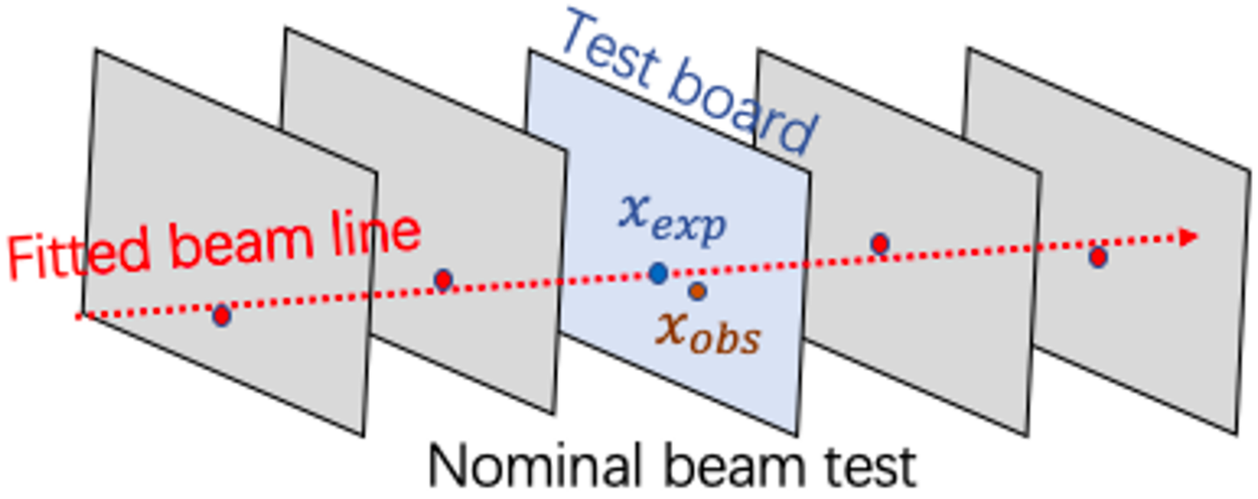
An example of wafer test result



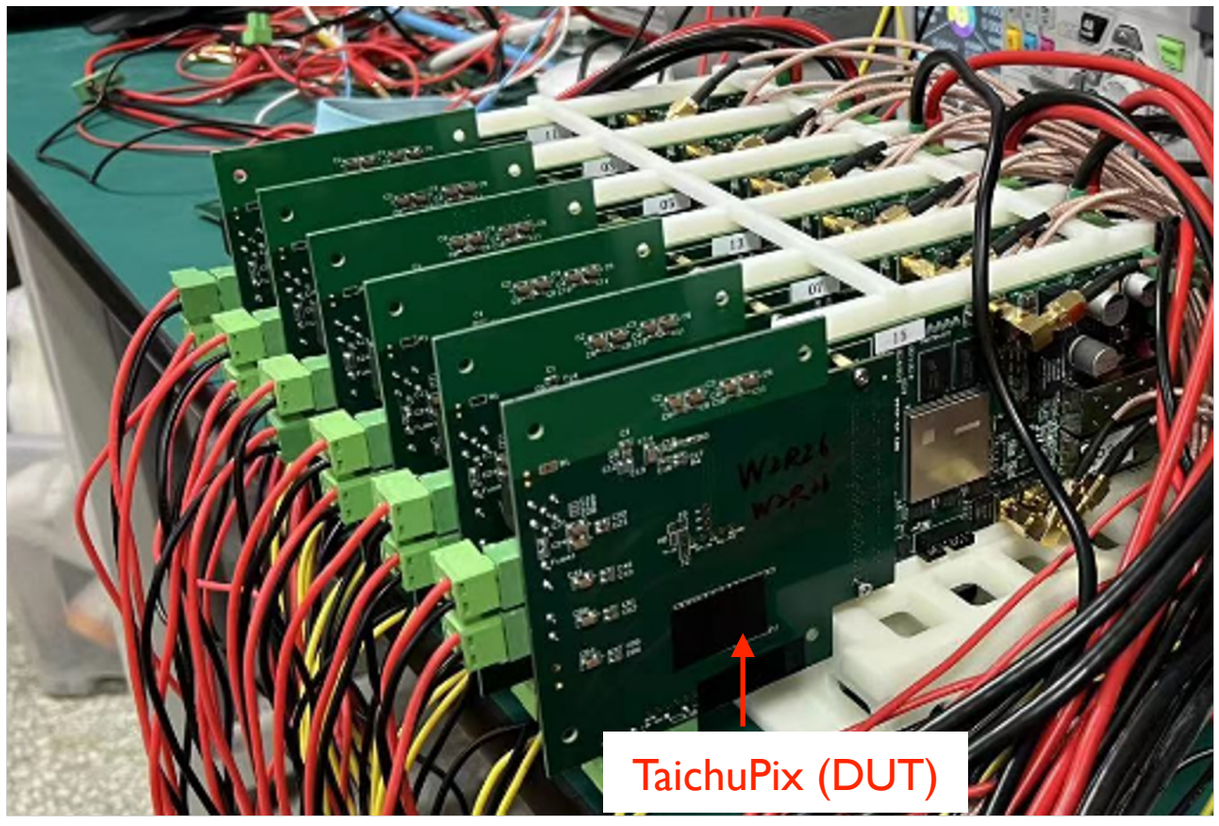
Link to Zhijun Liang's talk at the 2023 CEPC Nanjing workshop

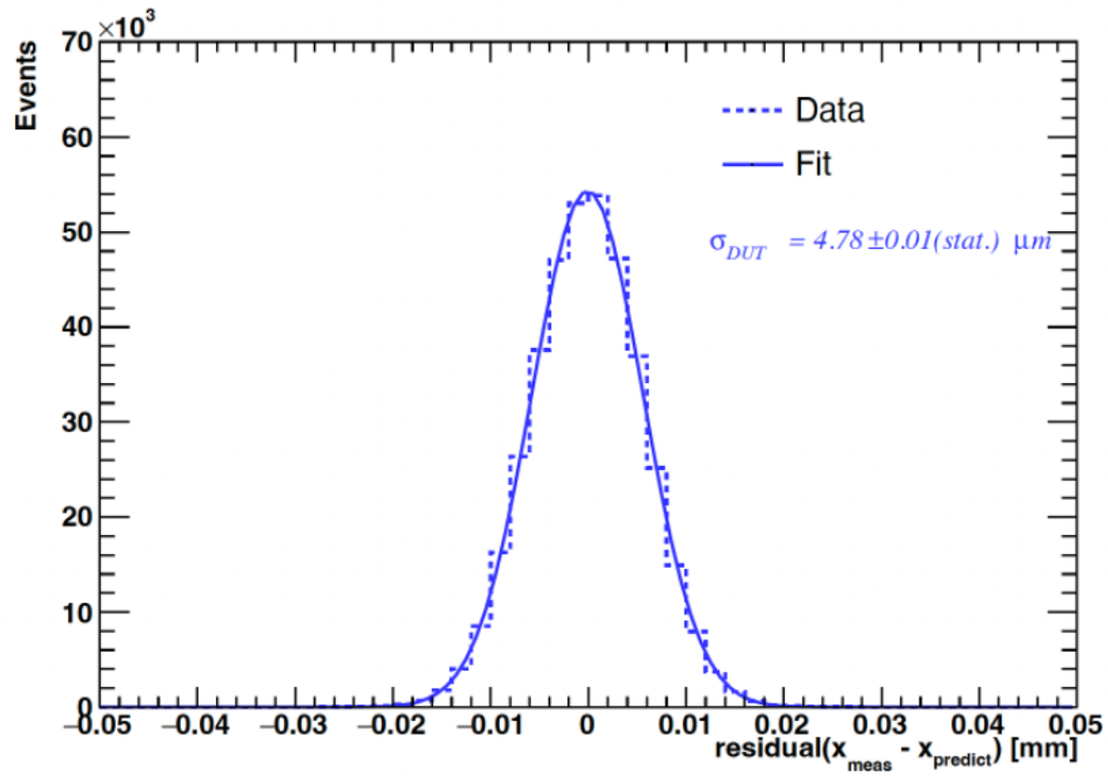
Test-beam results

- Two dedicated testbeams at DESY
  - 4-5 GeV electron beam
- Measurements
  - Spatial and timing resolutions, efficiencies



Meets the design 3-5um

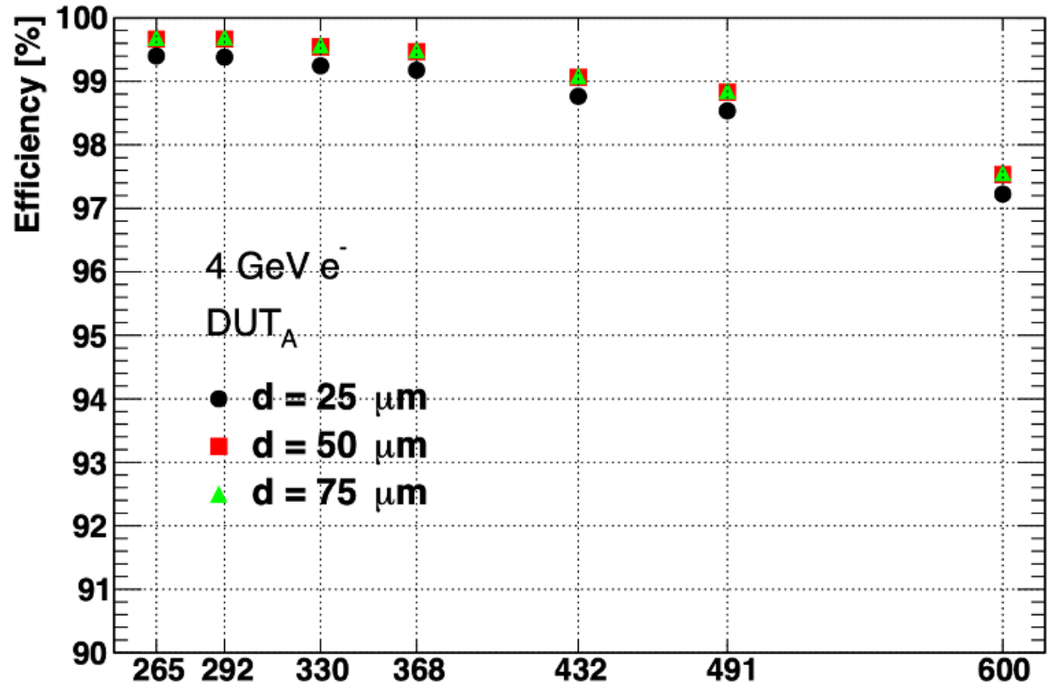


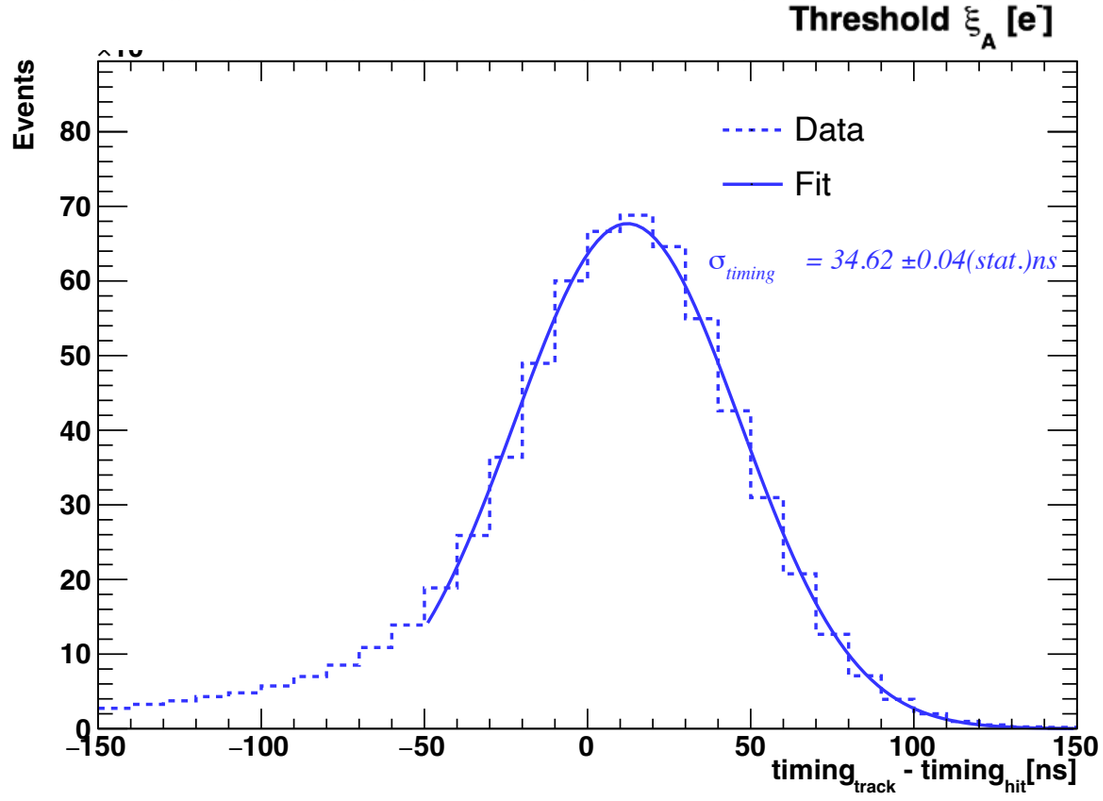


Link to Zhijun Liang's talk at the 2023 CEPC Nanjing workshop

TaichunPix3 efficiency and time

- Efficiency is the ratio of tracks that match the hit in the DUT within a given distance from predicted position extrapolated from telescope planes
  - ~99% for an optimised threshold
- CEPC time requirement is 25ns @40MHz Z pole collision
- TaichuPix telescope have 2 time stamps:
  - Time stamp from FPGA (all 6 Taichu chip synchronized by FPGA)
  - Precise time stamp from Taichu chip
  - By comparing telescope track time Vs DUT time, ~35ns @ 20MHz clock



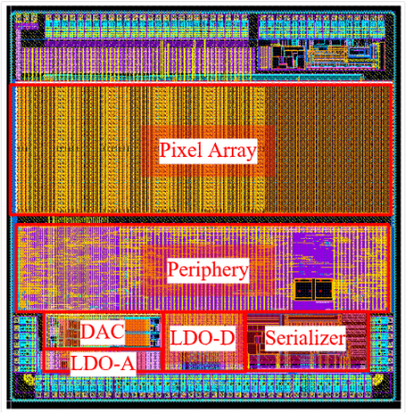


Link to Zhijun Liang's talk at the 2023 CEPC Nanjing workshop

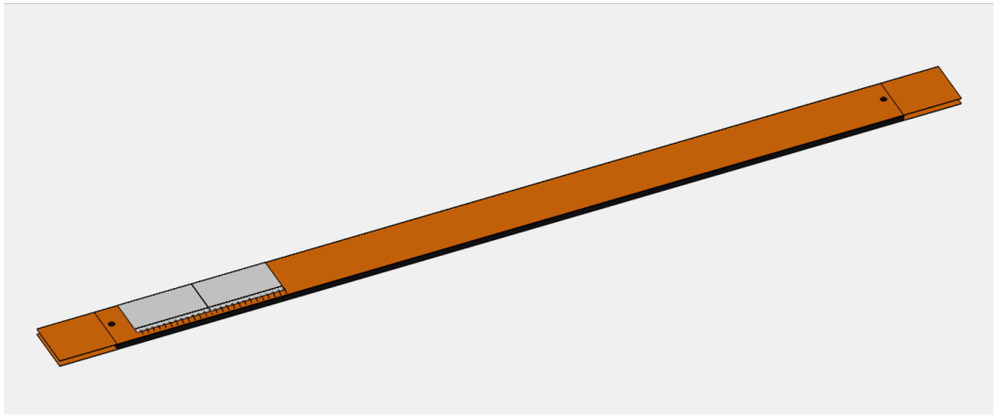
From sensor to system prototype

- R&D and prototyping in each step - an impressive achievement from nearly scratch

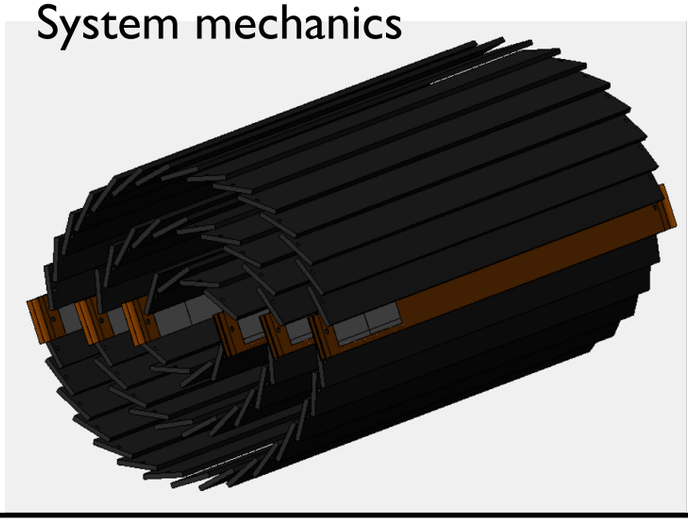
TaichuPix3

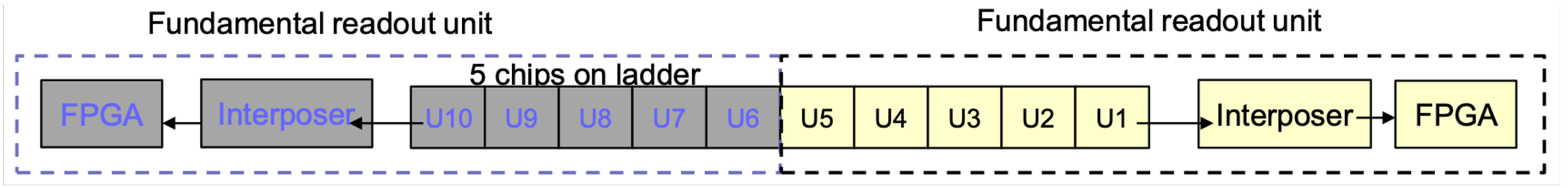


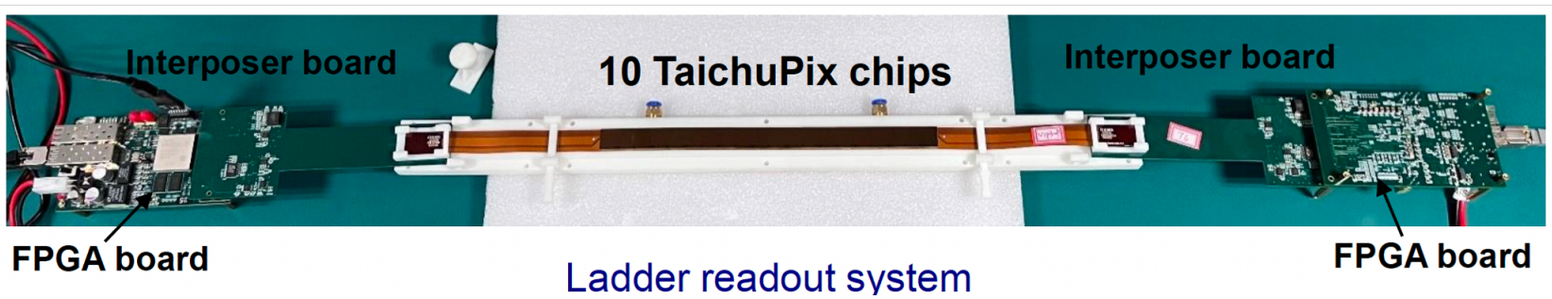
Ladder



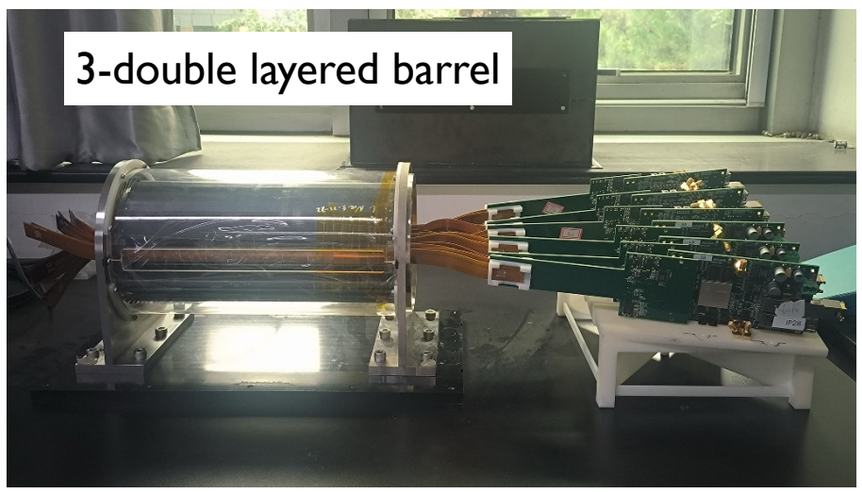
System mechanics







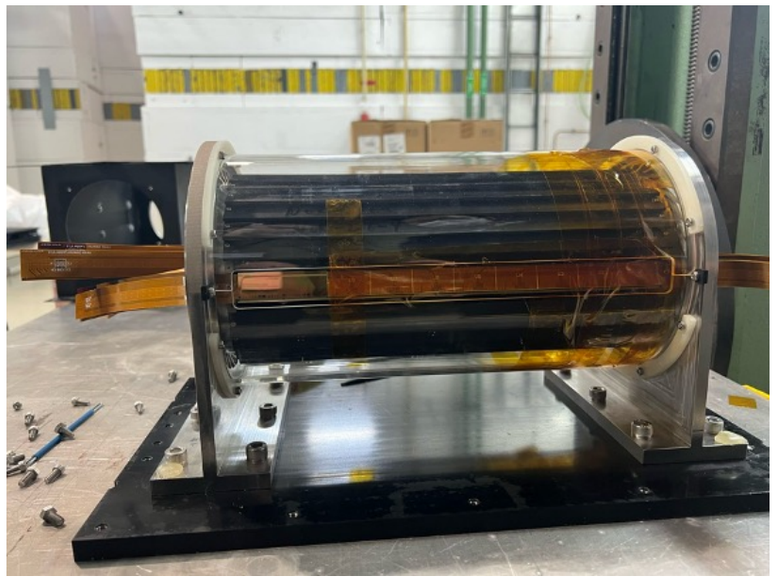
Ladder readout system

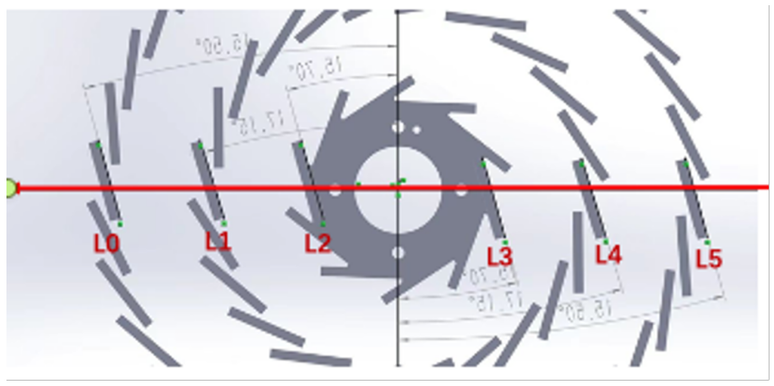


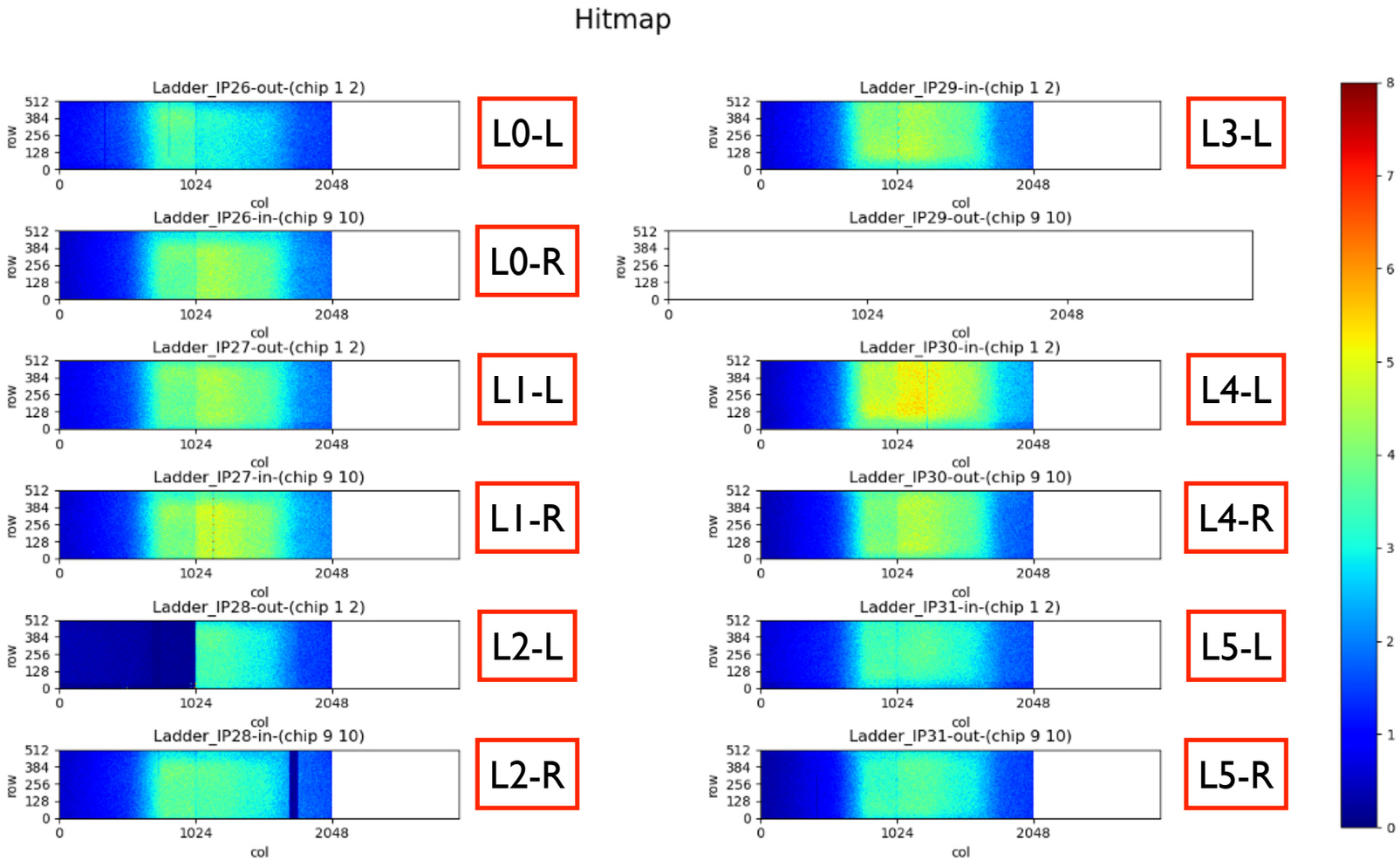
Link to Zhijun Liang's talk at the 2023 CEPC Nanjing workshop

Vertex detector prototype testbeam

- Six double-side ladders installed on the vertex detector prototype for DESY testbeam (Apr 2023)
  - 12 flex PCB , 24 TaichuPix3 chips installed on detector prototype
    - Full system mechanic support, population of sensor is ~ X% of the full detector
  - Beam spot (~2×2cm) is visible on detector hit map
  - Record about one billion tracks in two weeks



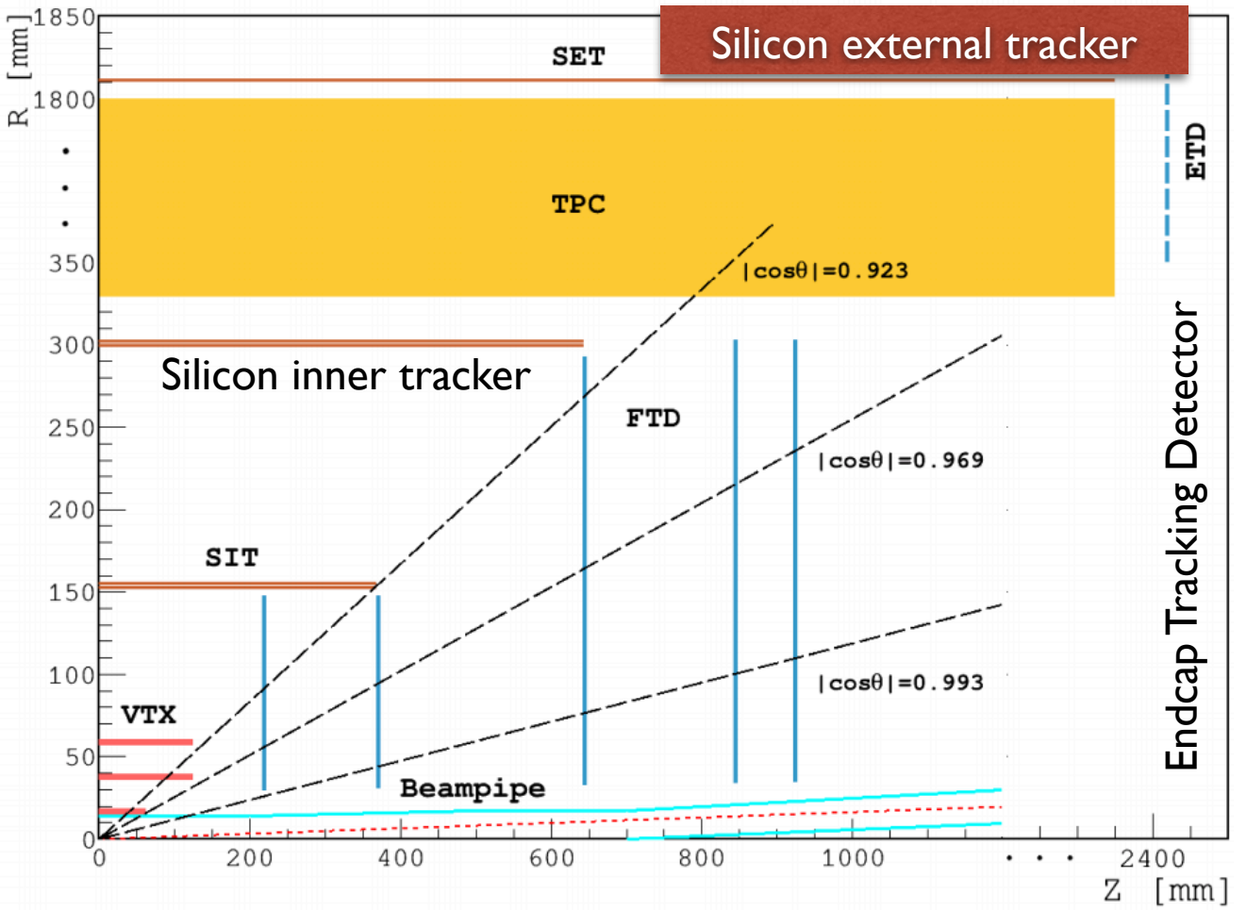




Link to Zhijun Liang's talk at the 2023 CEPC Nanjing workshop

Reminder of the CEPC Tracker requirements

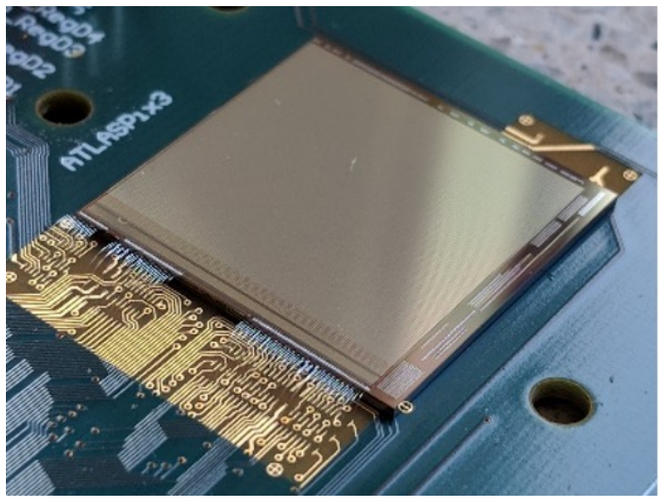
- Need to cover very large area O(70-140m^2), modest spatial resolution, 25ns timing (Z-pole)
  - Multiple scattering limits the bulk of the tracking performances

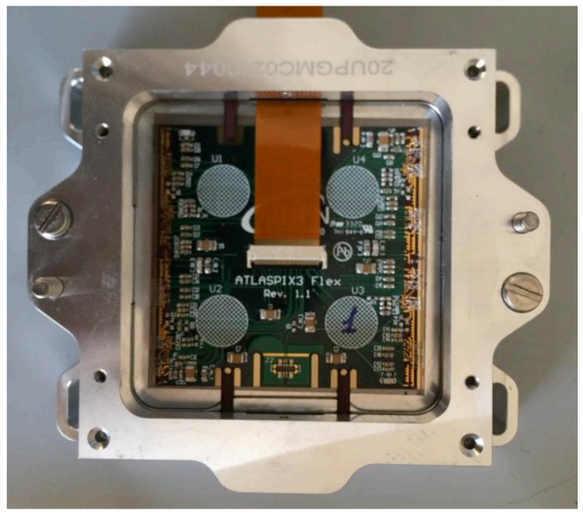


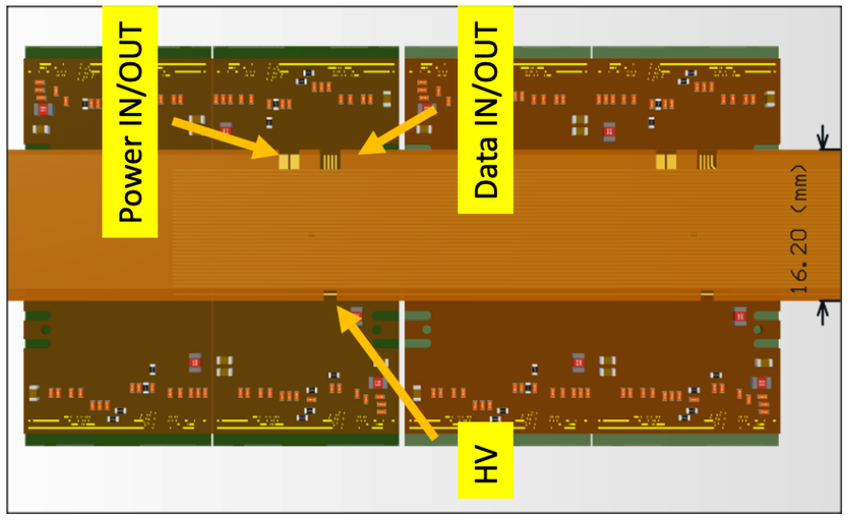
	Baseline CDR with TPC
Barrel	SIT-L1: R=0.15m, L=0.75m → A=0.7m^2 SIT-L2: R=0.3m, L=1.33n → A=2.5m^2 SET: R=1.8m, L=4.7m→ A=53m^2
Endcap	FTD D1-D5: 1.8 m^2 ETD: R_{out}=1.82m, R_{in} =0.42m → A=20 m^2
σ_{SP} (rϕ)	7 μm
σ_{SP} (Z)	Very loose ~ 100 μm
Timing	25 ns
Max* Occupancy	SIT-L1: 0.6%, SIT-L2: 10^{-3}, SET: 10^{-4}
Radiation	TID ~< 1kRad/year, NIEL ~< 10^{10} 1 MeV neq /cm^2. year
X/X_0	0.65% Barrel 0.5-0.65% Endcap

Overview of the silicon tracker R&D

- Silicon tracker R&D in the CEPC project has large international collaboration
  - A large effort focuses on system design and prototyping based on existing ATLASPix3 sensors (180nm TSI process) originally designed for ATLAS ITk pixel
    - Similar multi-chip module concept and serial powering schemes as the ATLAS ITk pixel
    - Mechanical support and cooling
    - A lot of the effort is common with FCC-ee and ATLAS ITk, see Attilio's slides
  - New sensor design is led by KIT, Prof Ivan Peric, exploring TSI 180nm/55nm foundries in China







List of research institutes with interest

- CEPC tracker R&D group (2019-), meeting every two weeks
  - Coordinators: Harald Fox (Lancaster) and Meng Wang (SDU)

- China
  - Institute of High Energy Physics, CAS
  - Shang Dong University
  - Tsinghua University
  - University of Science and Technology of China
  - Northwestern Polytechnical University
  - T.D.Lee Institute-Shanghai Jiao Tong University
  - Harbin Institute of Technology
  - University of South China
  - Hunan Univesity
  - Zhejiang University
  - Dalian Minzu University

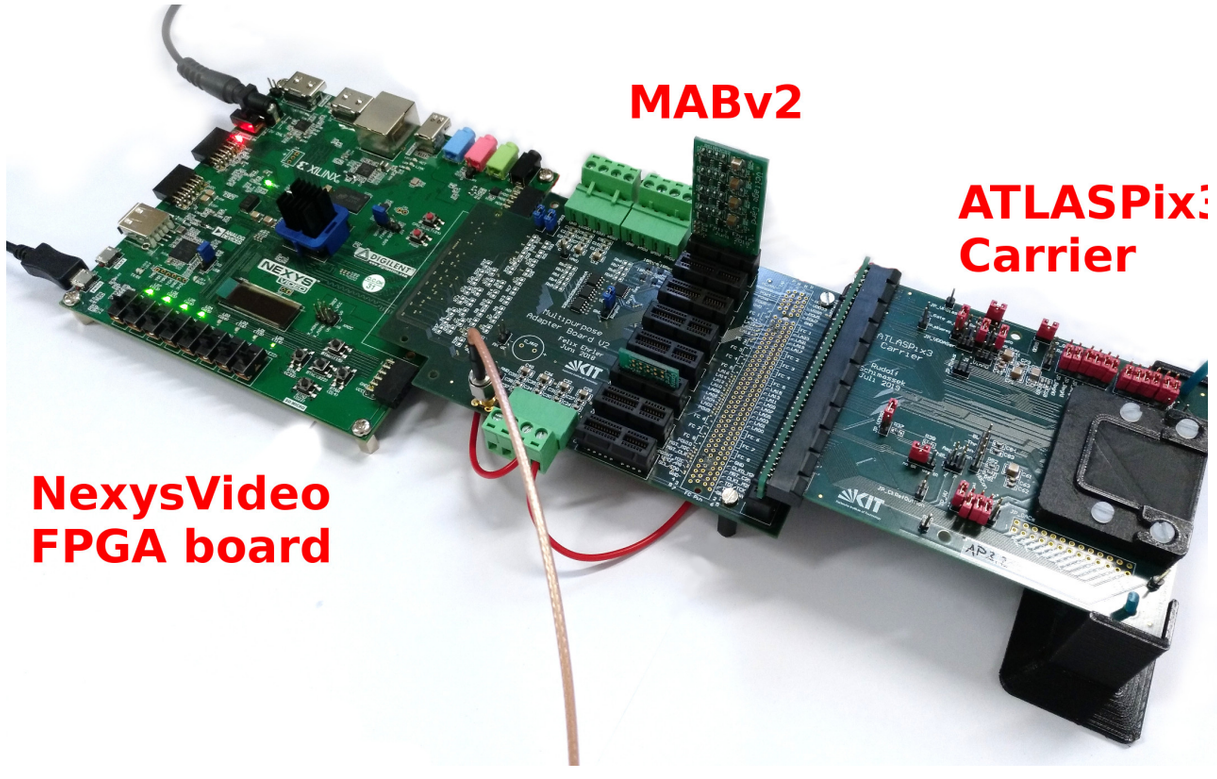
UK
- University of Bristol
- STFC-Daresbury Laboratory
- University of Edinburgh
- Lancaster University
- University of Liverpool
- Queen Mary University of London
- University of Oxford
- STFC-Rutherford Appleton Laboratory
- University of Sheffield
- University of Warwick

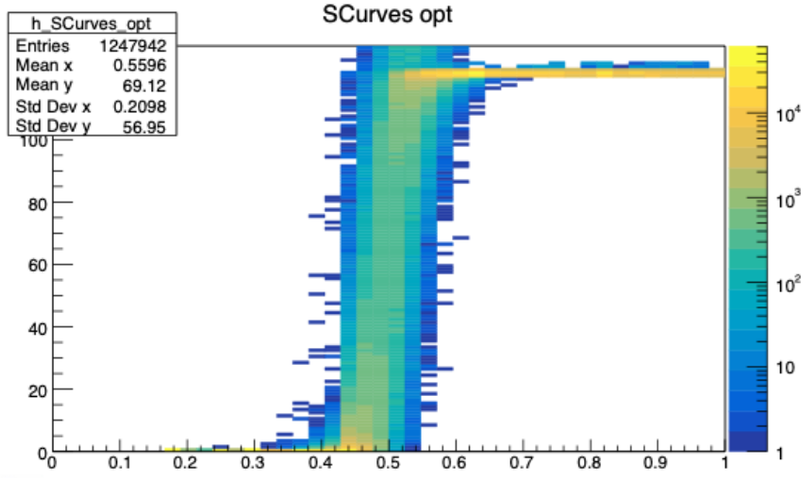
- Germany
  - Karlsruhe Institut für Technologie
- Italy
  - INFN Sezione di Milano, Università degli Studi di Milano e Università degli Studi dell'Insubria
  - INFN Sezione die Pisa, Università di Pisa
  - INFN Sezione di Torino, Università degli Studi di Torino
- Australia
  - University of Adelaide

ATLASPix3 programme overview

Karlsruher Institut für Technologie

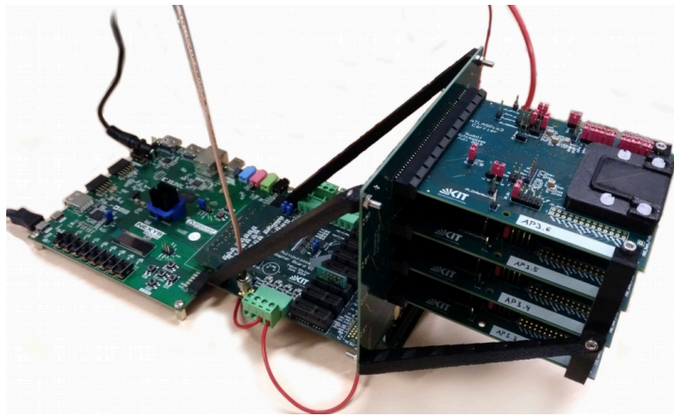
GECCO

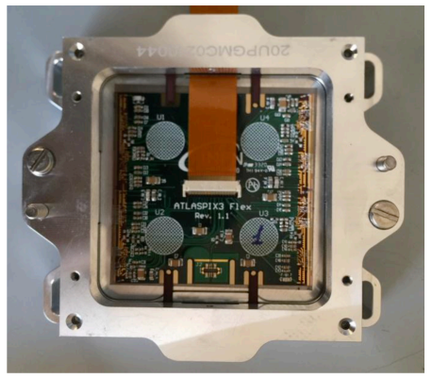




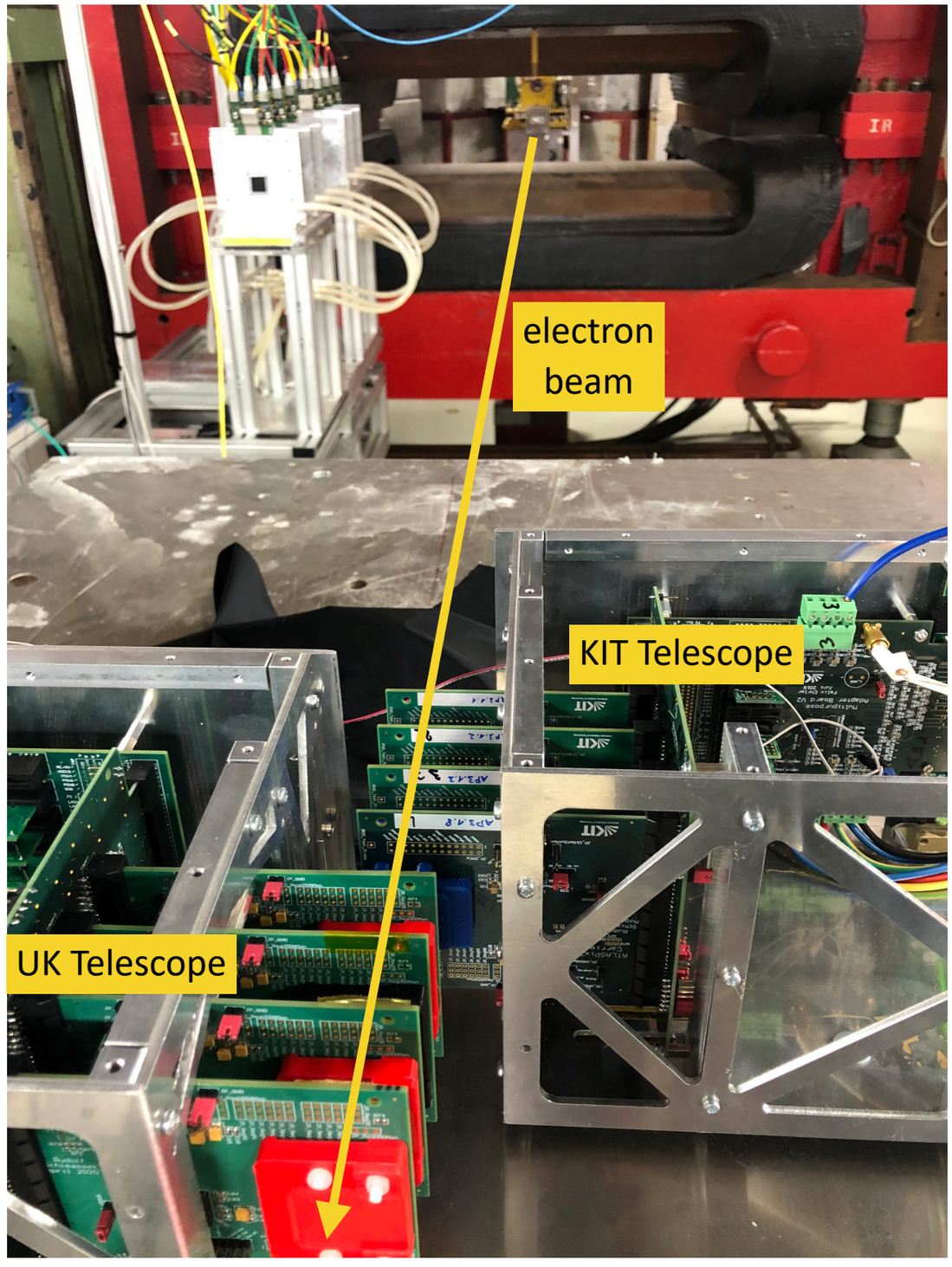
- 2 ATLASPix3.0 and 3 ATLASPix3.1 wafers diced (most thinned to 150um)
- O(65) GECCO boards and single chip carriers produced in China and distributed globally
  - Many institutes commissioned single chip lab test setup and performed electrical measurements
- A four-chip quad module is designed, manufactured, and tested using ATLASPix3.0 chips
  - 2nd version of module flex is designed for ATLASPix3.1 to study Serial Powering
- Successful testbeam at DESY in April 2022: two ATLASPix3.1 telescopes and one quad

Telescope and DESY Test Beam





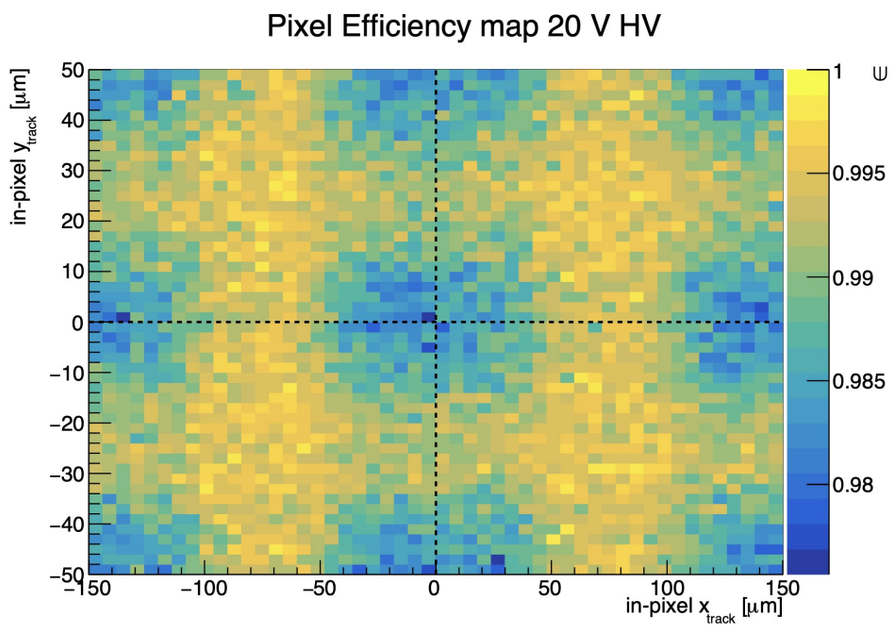
- Testbeam at DESY April 2022
  - Lancaster, KT, Milano, KIT, Bristol, Edinburgh, RAL
- Two 4-layer telescopes and a quad tested
- Readout and reconstruction:
  - Hit driven readout
  - Reconstruction with Corryvreckan
  - Iterative alignment of the layers
  - Tracking through 3 or 4 layers
  - An arbitrary layer can function as DUT, here layer 3 is used as DUT

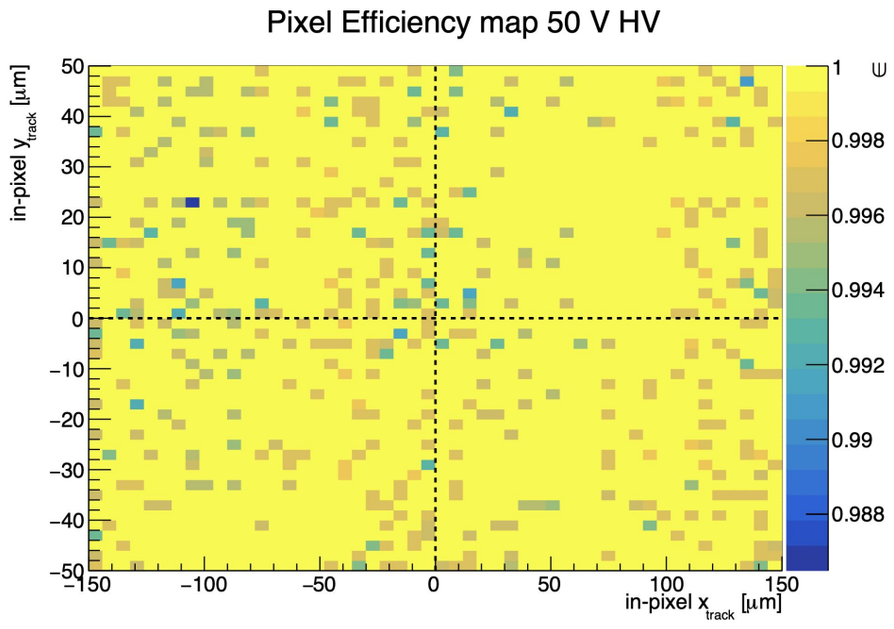


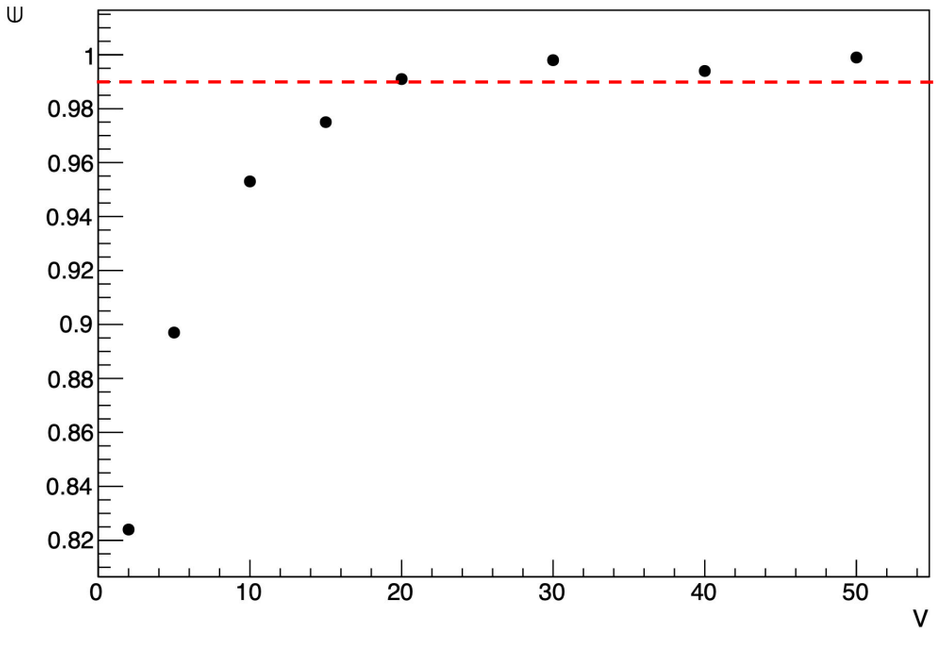
Link to Harald Fox's talk at the 2023 CEPC Nanjing Workshop

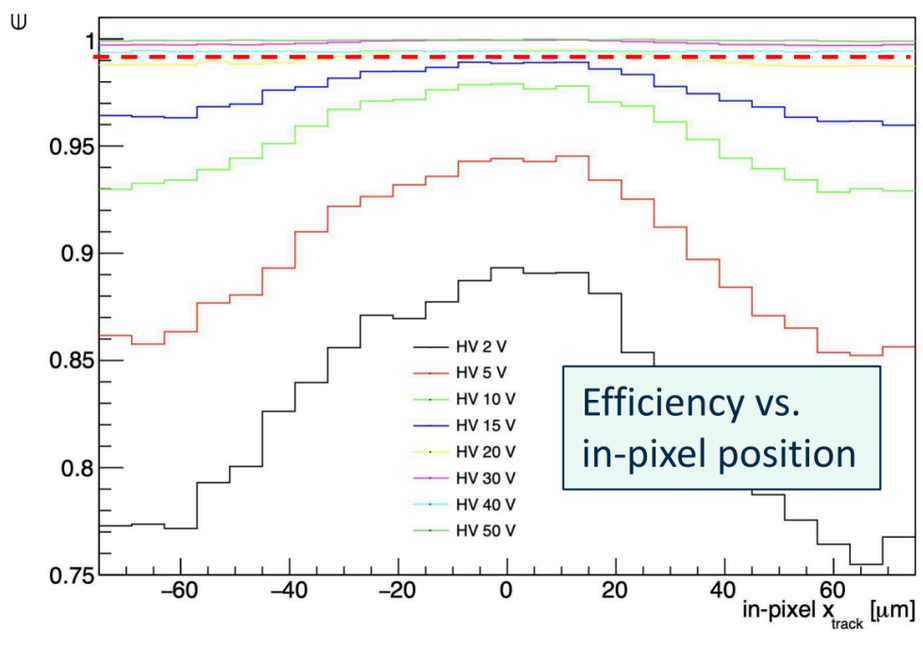
Testbeam results

- Efficiency > 99% and uniform in the detector for depletion voltages >20 V
- Position resolution in the 10-11 μm range







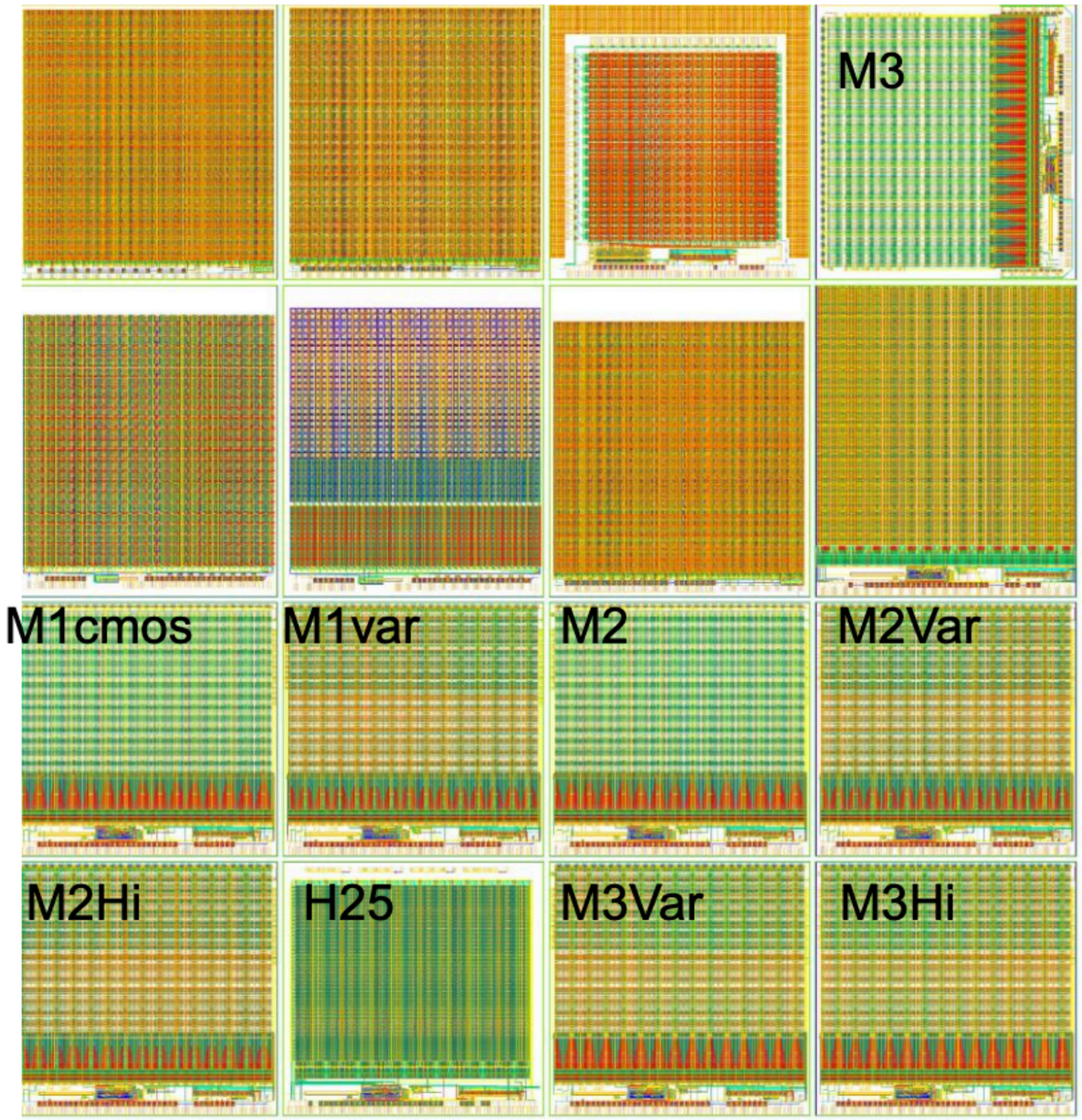


Link to Harald Fox's talk in 2023 CEPC Nanjing Workshop

Sensor improvements: TSI 180nm

Karlsruher Institut für Technologie

- Engineering run 2020 and 2021
  - TSI 180nm
  - Several designs: CLIC, CEPC, DESY telescope upgrade (TELEPIX)
  - Pixel 25um ×165 um
- Improvements beyond ATLASPix3
  - Improved breakdown voltage by better design of guard ring (60V → 120V)
  - Reduction of power consumption by optimized amplifier and comparator designs



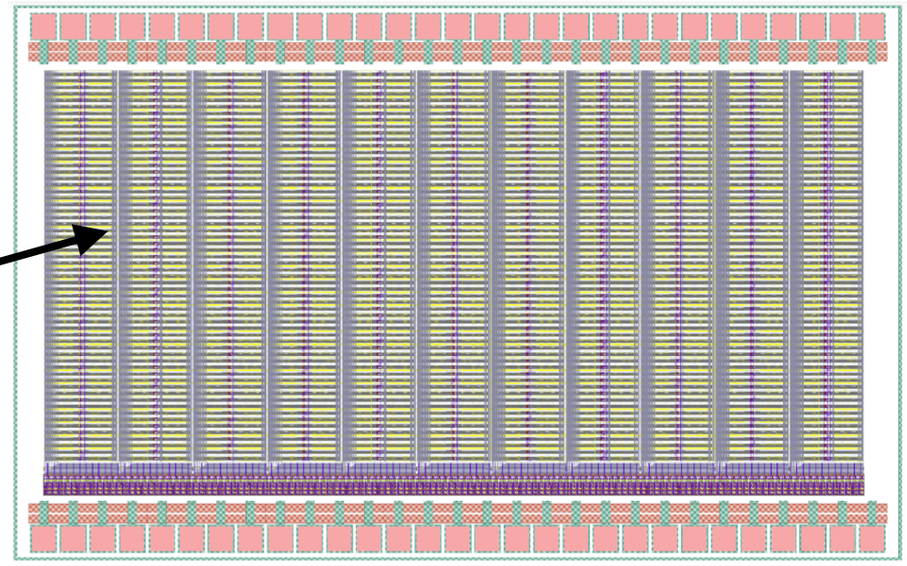
https://adl.ipe.kit.edu/english/26.php

Link to Ivan Peric's talk at the UK-CEPC tracker workshop Nov 2021

CMOS 55nm Technology with Chinese foundaries

- Design and fabrication with two Chinese foundries using 55nm technology
  - Sensor design effort led by KIT and IHEP
- A couple of submission attempts with HLMC
  - high-resistance substrate not yet supported
  - MPW cancelled by foundary in 2022 due to covid

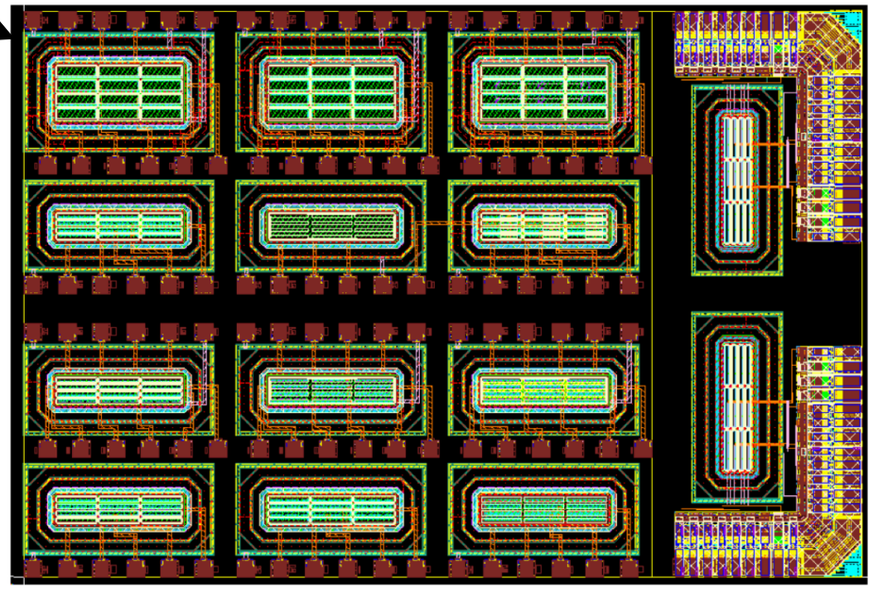
HLMC 上海华力微电子有限公司 Shanghai Huali Microelectronics Corporation



- Non-HV MPW at SMIC 5 in Oct 2022
  - Done with low leakage process,
  - 40 chips delivered in Apr 2023, tests are on-going initial results promising
- First HV MPW submitted to SMIC in Aug 2023
  - Based on High-res wafer of 1k Ωcm

Ivan Peric et al

SMIC 中芯国际集成电路制造有限公司 Semiconductor Manufacturing International Corporation



Link to Yiming Liu's talk in 2023 CEPC Edinburgh workshop

HV-CMOS 55nm at SMIC

SMIC 中芯国际集成电路制造有限公司 Semiconductor Manufacturing International Corporation

KIT
Beijing IHEP
Shandong University
Hunan University
Dalian Minzu University
Zhejiang University

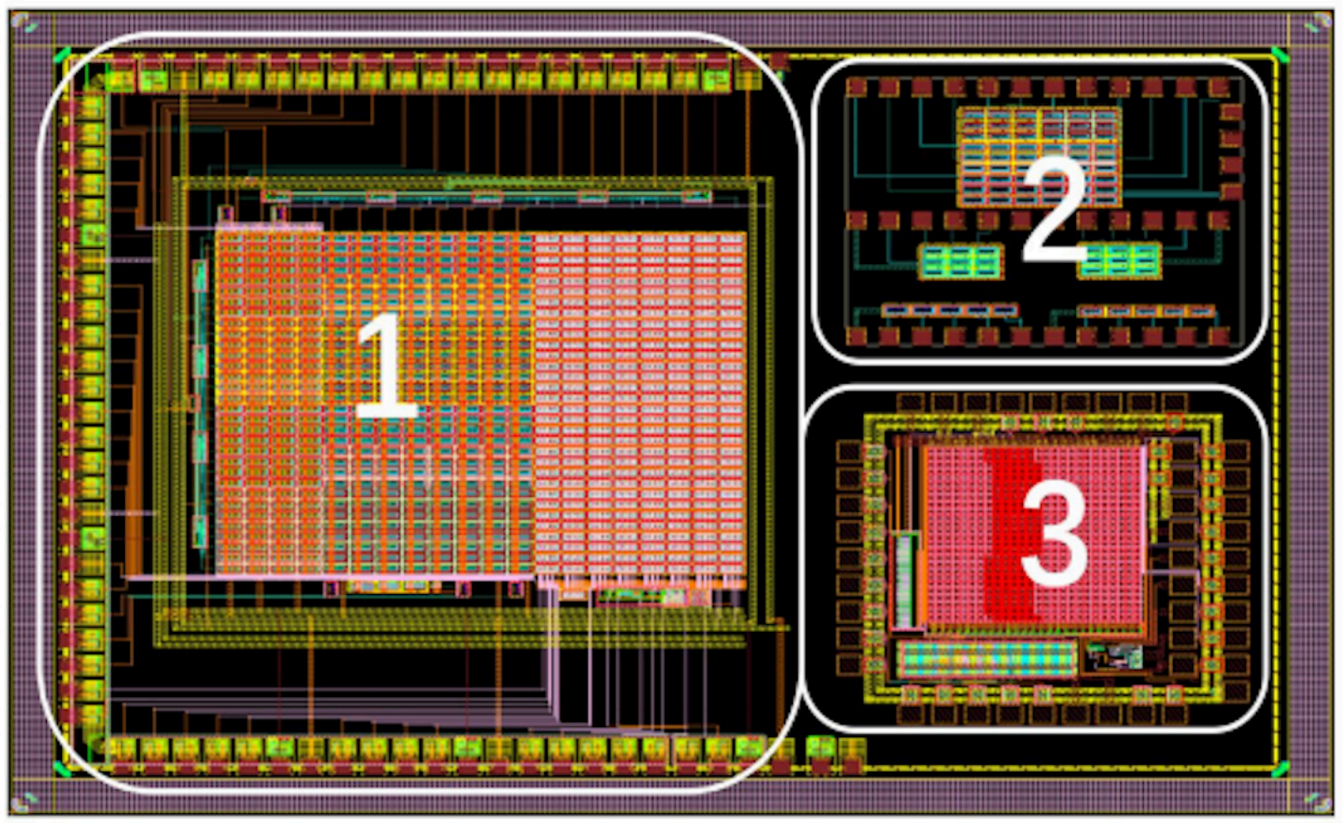


Figure: layout of the first submission on the 55nm HV-CMOS process. 3 independent sections are included for different purpose. The whole chip size is 4mm×3mm.

- 1st section: a 32×20 pixel matrix comprises various diodes and in-pixel amplifier and discriminator design for process validation;
- 2nd section: 5 diode array for charge sensing diodes I-V/ C-V study;
- 3rd section: a 26×26 pixel matrix with relative digital readout periphery for new electronics structure study; (Hui Zhang's talk & Ruoshi Dong' poster)

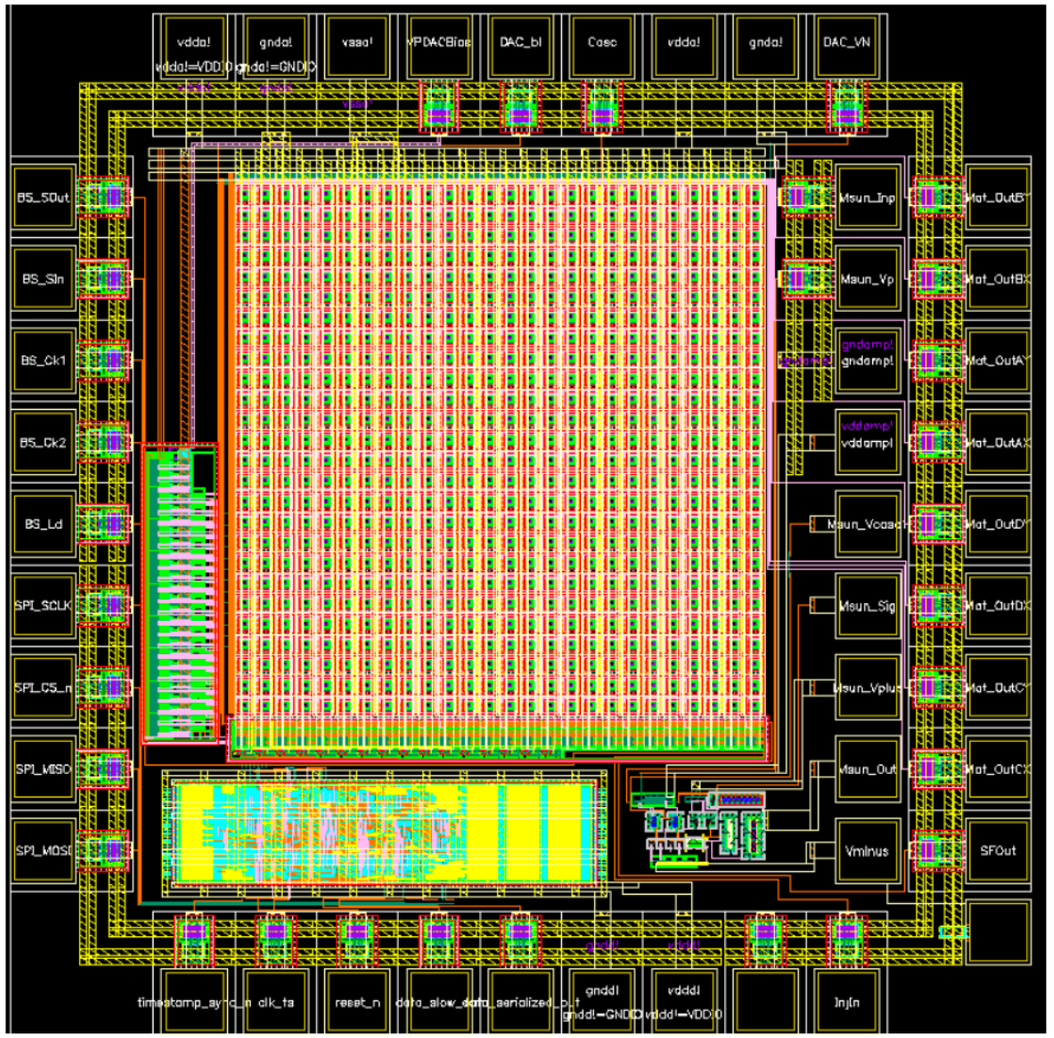
SMIC 55nm HVCMOS - CEPCPix1

Karlsruher Institut für Technologie

中芯国际集成电路制造有限公司
Semiconductor Manufacturing International Corporation

- Implemented in 55nm process
- Submitted in August 2023
- Chip size: ~ 1.25 mm × 1.25 mm
- Pixel matrix: 26 columns (2 digital + 24 analog), 26 rows
- Pixel:
  - 25 μm × 25 μm
  - PMOS amplifier and NMOS comparator
- Bias voltages:
  - Integrated 8-bit voltage DACs
  - Can be supplied externally

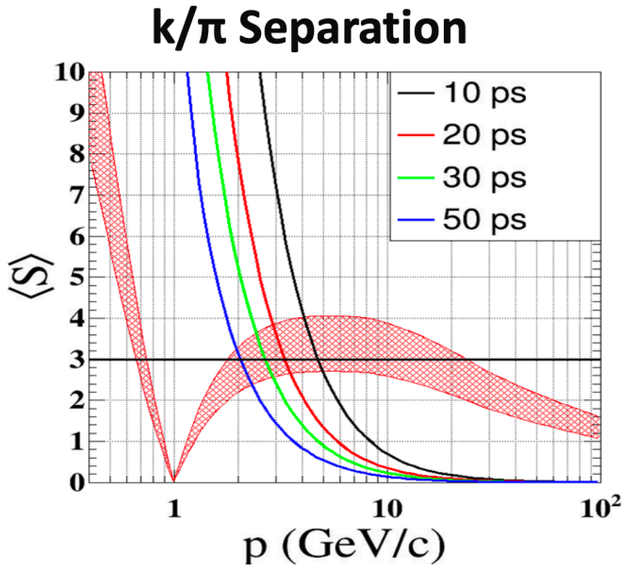
Third section

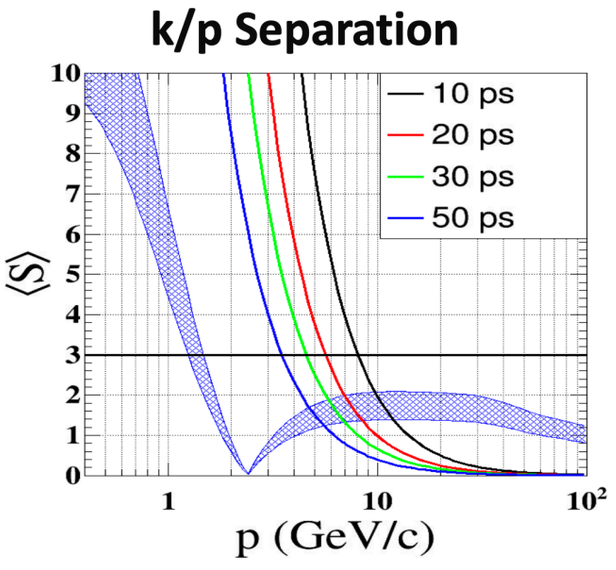


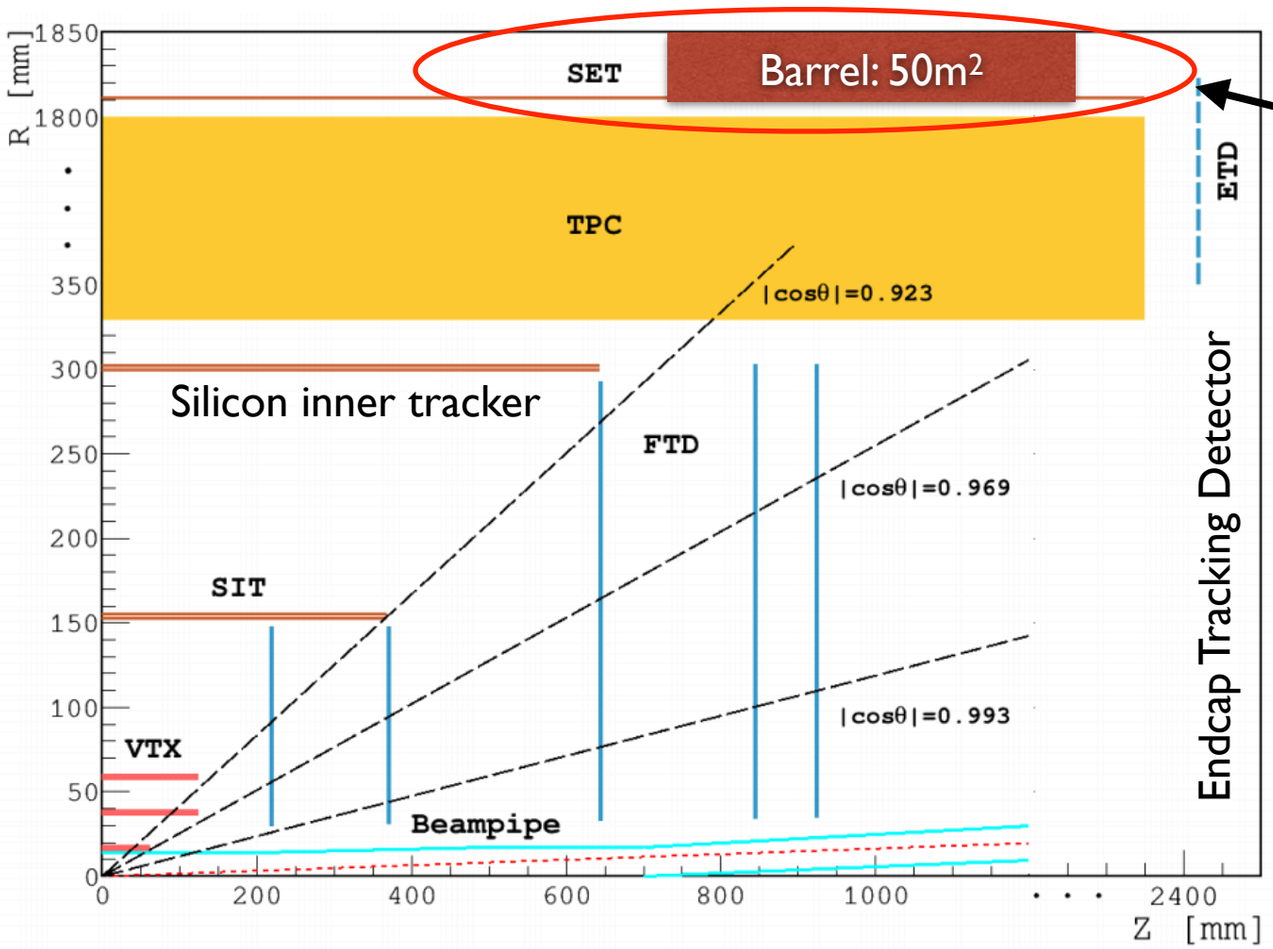
Talk by Hui Zhang (KIT) in CEPC 2023 Workshop in Nanjing

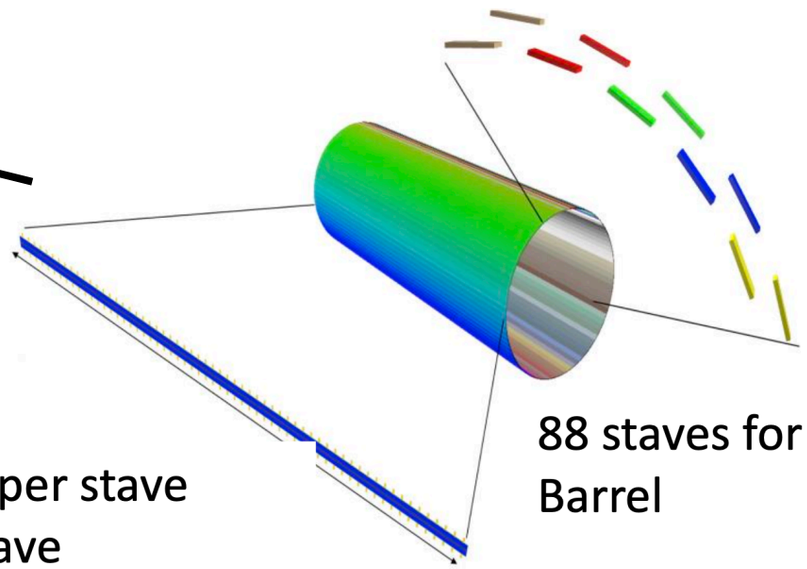
LGAD for Time-of-Flight detector layer

- Precision timing layer for PID, one of the key recommendations from the CEPC IAC
  - Important for the flavour physics, especially at the Z-pole running (10^{12} Zs!)
- Part of the SET (silicon wrapper layer outside of either TPC or DCH)









60 modules per stave
2.4 m per stave

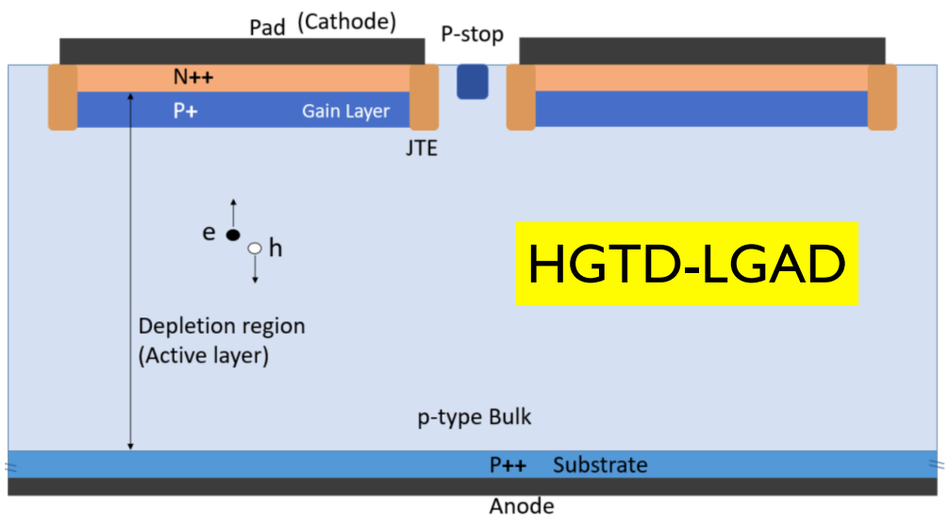
88 staves for the Barrel

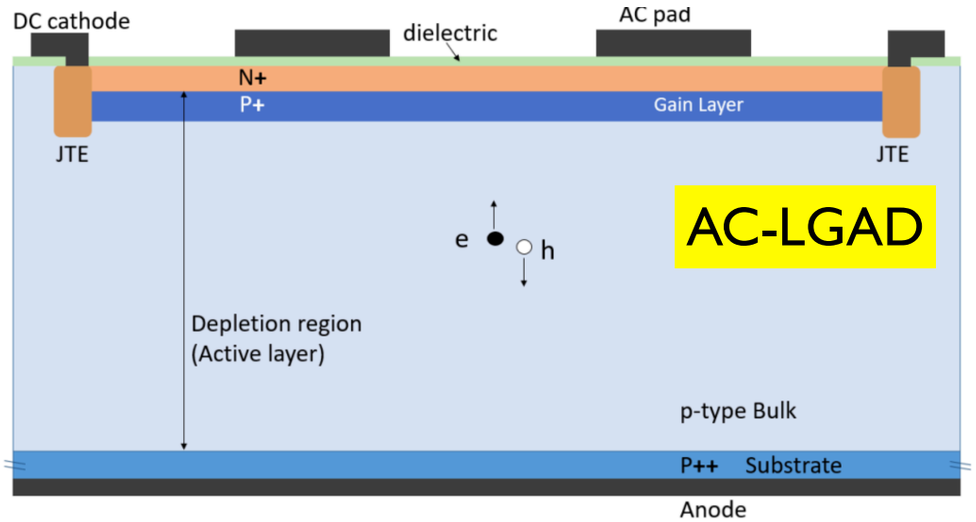
Time resolution: 30-50ps, Spatial resolution: 10um
Strip-like sensor (4cm*0.1cm)

Link to Mei Zhao's talk in 2023 CEPC Nanjing workshop

AC-LGAD sensor designs

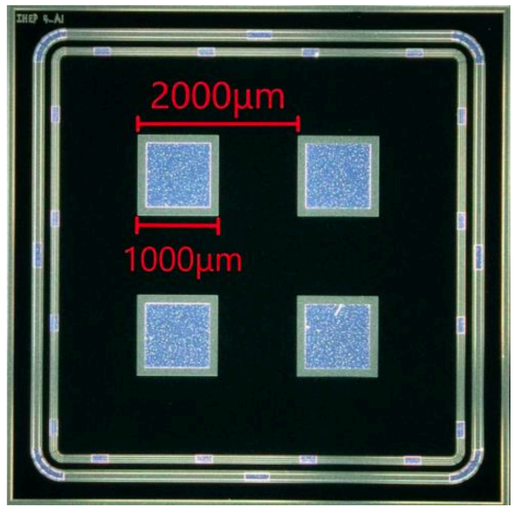
- Building upon China's leading role at the ATLAS TGTD project
  - 2023 IHEP-IME got all the share of the order from CERN tendering of about 10,000 LGAD
- CEPC designs are based on AC-LGAD (no dead zones), synergy with EIC proposal





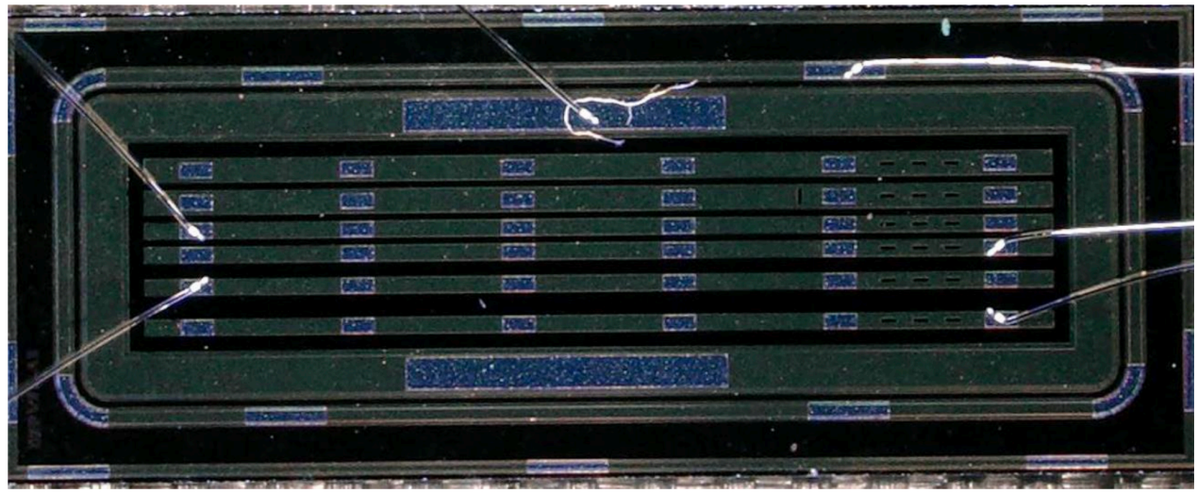
Pixel AC-LGAD

IHEP
AC-LGAD



Different process parameters:
n+ dose(phosphorus): 10P to 0.2P

Strip AC-LGAD: strip length 5.6mm



Pitch-pad: 250-100um, 200-100um, 150-100um

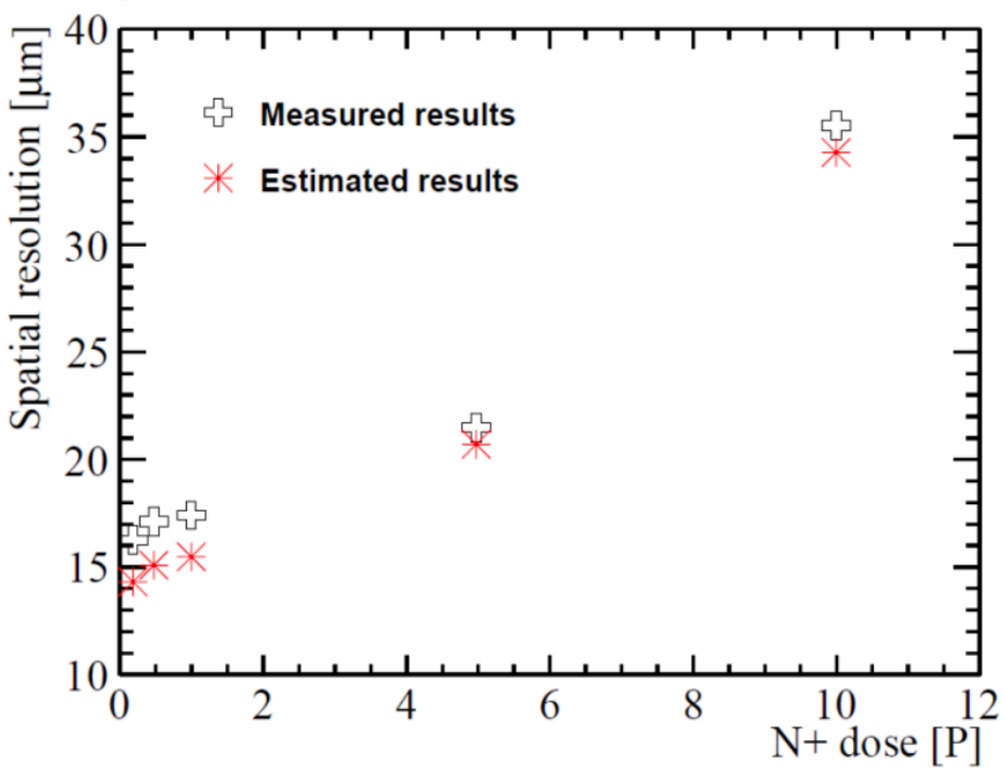
Link to Mei Zhao's talk in 2023 CEPC Nanjing workshop

Spatial resolution

- Spatial resolution target can be reached

Pixel AC-LGAD: (pitch-pad: 2mm-1mm)

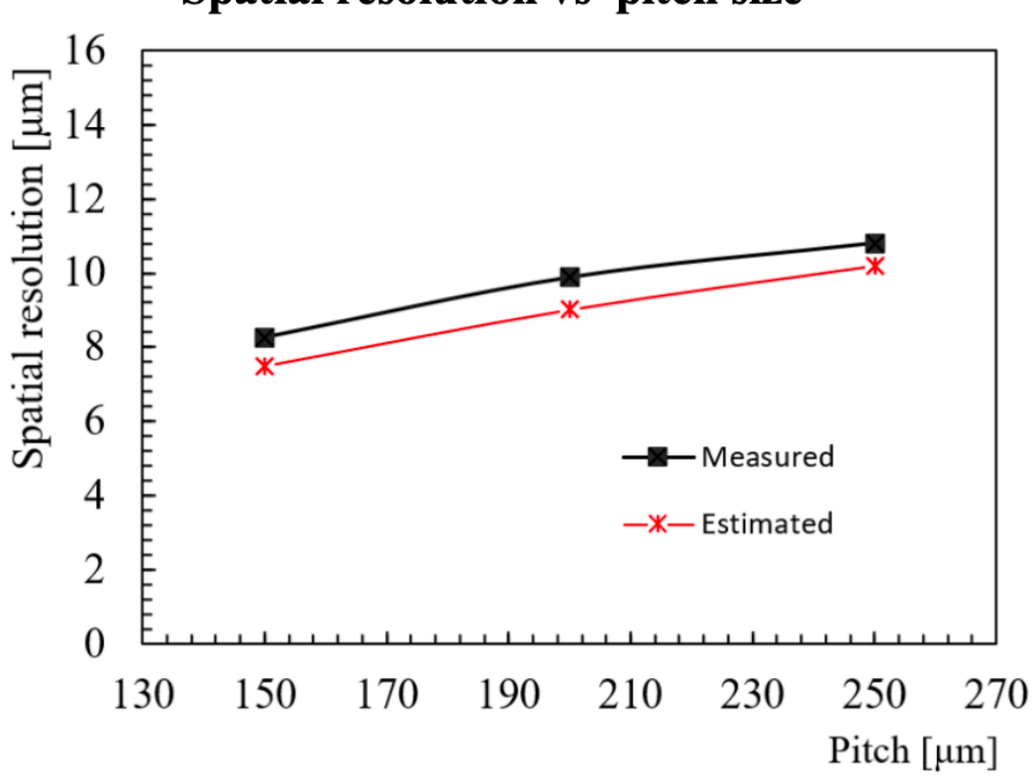
- 10 P → 0.2 P, spatial resolution reduce to 15um



Strip AC-LGAD:

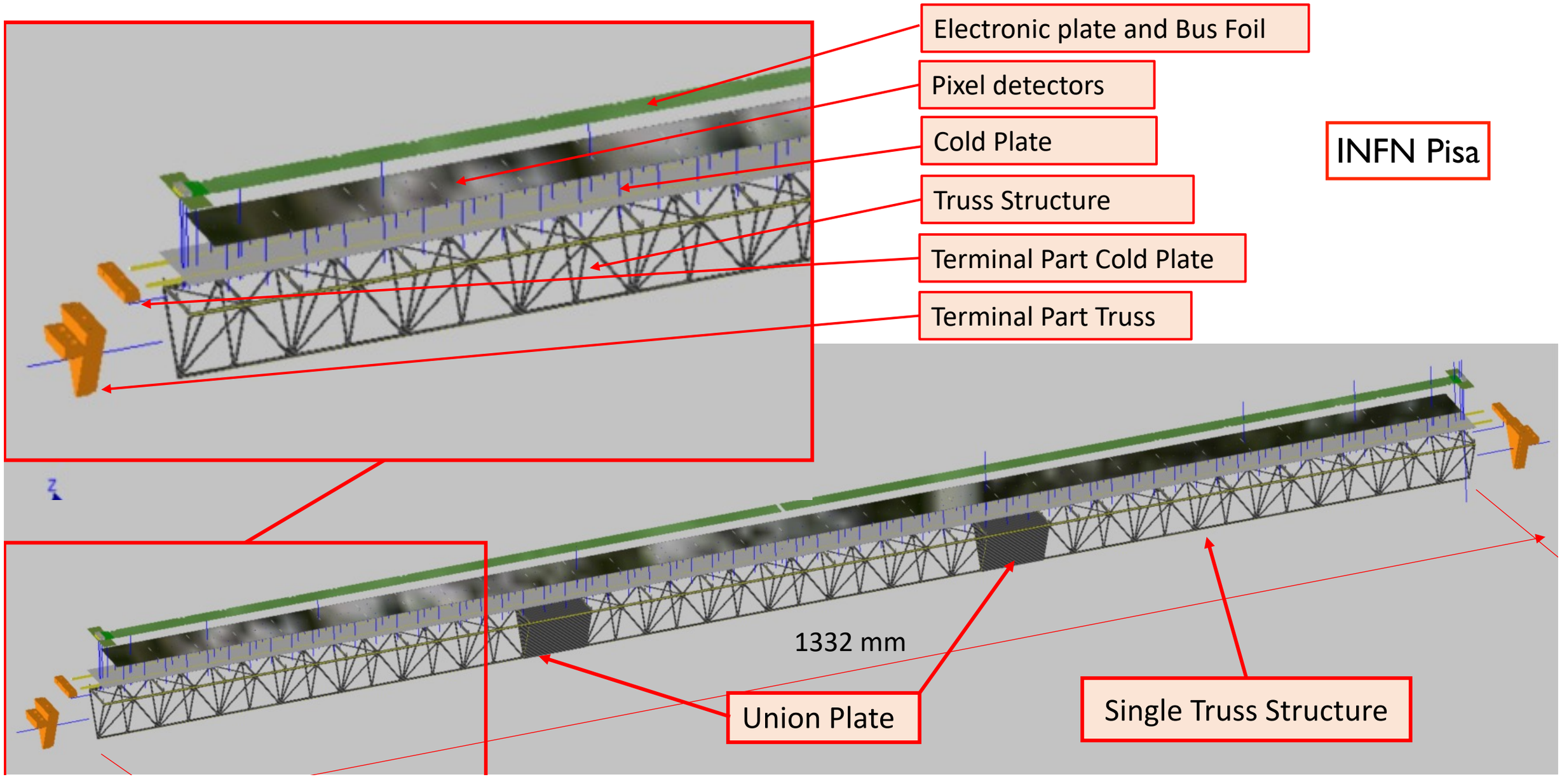
(pitch-pad: 250-100um, 200-100um, 150-100um)

Pitch size 250um →150um, spatial resolution 11→ 8 μm



Mechanical R&D: Long stave design

- Dedicated CEPC design and prototyping for mechanical support for SIT Layer 2

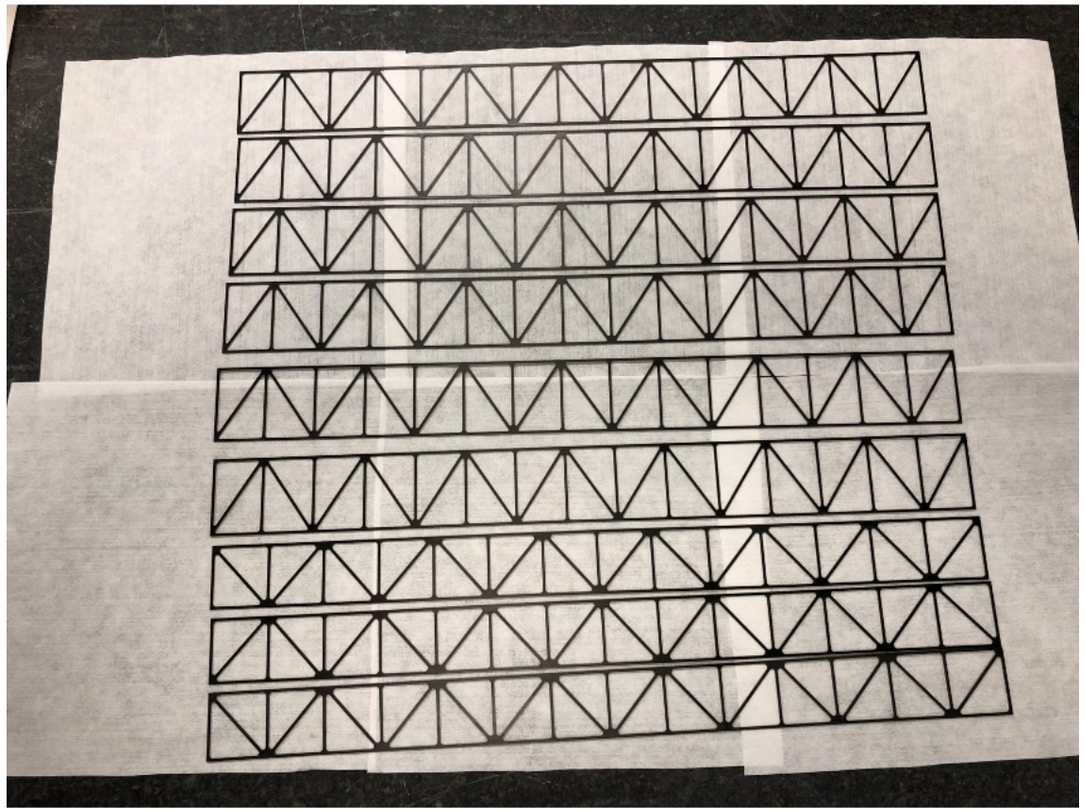


Link to Filippo Bosi's talk in 2023 CEPC Edinburgh workshop

Mechanical R&D: single truss structure prototyping

INFN Pisa

Single truss structure realized by WaterJet industry
Special process waterjet technology (precision 50 micron)



LAMINATED FOIL

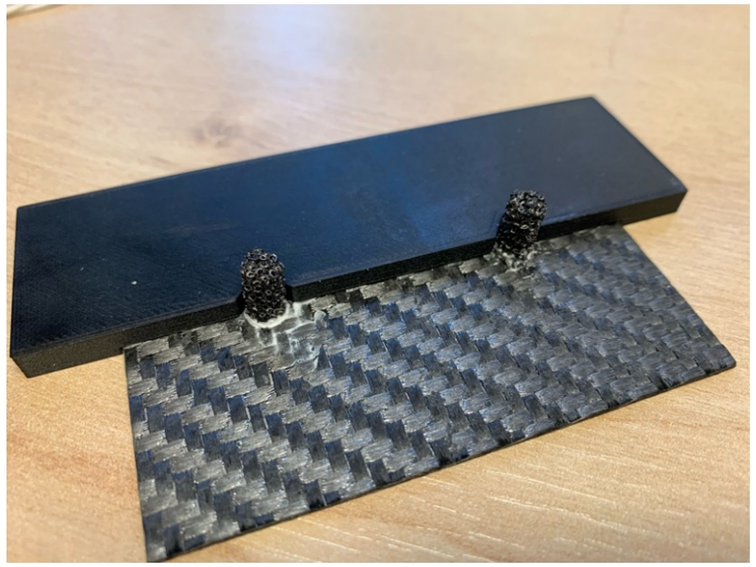
Th=0,5 mm of 550x460 mm2

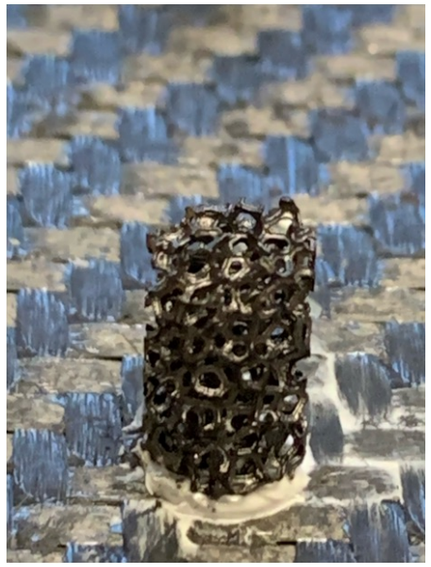
Carbon Fiber MJ46

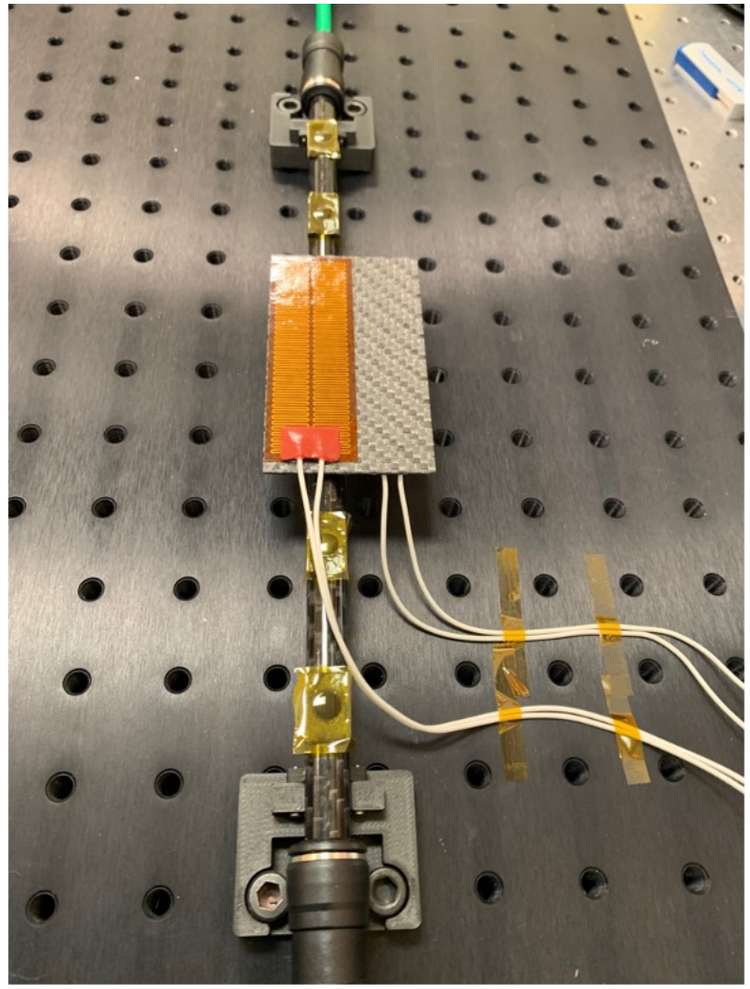
Link to Filippo Bosi's talk in 2023 CEPC Edinburgh workshop

Pre-prototype thermal evaluations

Pre-prototype: Base attached to tube & heaters on







- Investigate performance of high-thermal conductivity (eg Allcomp) foams as a heat exchanger
  - Combination of large area and increased stream velocity through foam can lead to high efficiency
- Characterise performance (i.e. temperature rise vs power) for different flow velocities
- Develop FEA models simulating the fluid flow through foams

*First look: at 3.1W power (expected from 8cm*4cm area), temperature rise ~10 degrees w.r.t. CDA*

Liverpool

T. Jones: UK-CEPC SiTracker Meeting Nov 2021

Summary

- The CEPC project values and welcomes international collaboration
  - Vertexing and tracking detectors in particular are of high interest for UK community
- The CEPC Chinese community prioritise the sensor R&D for the vertex detector
  - A full size CMOS sensor sensor TaichuPix3 (TowerJazz 180nm CIS process) ER-2022
  - TaichuPix3 has reached the designed spatial resolution (not far from the time resolution)
- For the central area tracking detectors, both gaseous and silicon solutions are proposed
- HV-CMOS continue to drive the central tracking R&D effort
  - Large international effort on system design based on existing ATLASPix3 sensors
    - First quad module constructed and evaluated - significant step towards large area application
    - Prototyping for mechanic and cooling are being pursued
  - KIT is leading the design effort for new sensors
    - First HVCMOS MPW submitted with Chinese foundries SMIC Aug 2023
- LGAD building upon ATLAS HGTD effort is ramping up as ToF technology

Backup slides

CEPC current plan and schedule

From Yuhui Li's CEPC overview talk

A CAS committee currently evaluates major accelerator options in China

CEPC is ranked top based on a list of criteria that includes scientific significance, strategic values and the readiness of design, R&D and engineering capabilities.

A final report will be submitted to CAS for consideration for the 15th 5-year-plan (2026-2030).

CEPC will propose to the government to begin construction around 2027-8 during the 15th 5-year-plan period.

Input from director of IHEP Yifang Wang

- *CEPC projects welcomes and values international collaboration*
- *International collaboration is considered key to the success of the fund application*
- *China has, and will continue to, contribute to other global particle physics projects*

CEPC operation plan

- Latest TDR has a 18 year operation planned
  - Z-pole data-taking drives the detector requirements (2T) due to the high rates and lumi

Particle	Ec.m. (GeV)	Years	SR Power (MW)	Lumi. /IP ($10^{34}cm^{-2}s^{-1}$)	Integrated Lumi. /yr (ab^{-1}, 2 IPs)	Total Integrated L (ab^{-1}, 2 IPs)	Total no. of events
H*	240	10	50	8.3	2.2	21.6	4.3×10^6
			30	5	1.3	13	2.6×10^6
Z	91	2	50	192**	50	100	4.1×10^{12}
			30	115**	30	60	2.5×10^{12}
W	160	1	50	26.7	6.9	6.9	2.1×10^8
			30	16	4.2	4.2	1.3×10^8
$t\bar{t}$	360	5	50	0.8	0.2	1.0	0.6×10^6
			30	0.5	0.13	0.65	0.4×10^6

From Yuhui Li: CEPC workshop Nanjing 2023

Key accelerator parameters

The Evolution: from CDR to TDR

Main Parameters (30MW)

CDR（2018）

	Higgs	*W*	*Z（3T）*	*Z（2T）*
Number of IPs	2			
Circumference (km)	100			
Bunch number	242	1524	12000	
β function at IP β_x^* / β_y^* (m/mm)	0.36/1.5	0.36/1.5	0.2/1.5	0.2/1.0
Emittance $\varepsilon_x/\varepsilon_y$ (nm/pm)	1.21/3.1	0.54/1.6	0.18/4.0	0.18/1.6
Energy acceptance (%)	1.35	0.4	0.23	
Luminosity per IP ($10^{34}cm^{-2}s^{-1}$)	**2.93**	**10.1**	**16.6**	**32.1**

TDR（2023）

	Higgs	*W*	*Z (2T)*	*ttbar*
Number of IPs	2			
Circumference (km)	100.0			
Bunch number	268	1297	11934	35
β functions at IP β_x^*/β_y^* (m/mm)	0.3/1	0.21/1	0.13/0.9	1.04/2.7
Emittance $\varepsilon_x/\varepsilon_y$ (nm/pm)	0.64/1.3	0.87/1.7	0.27/1.4	1.4/4.7
Energy acceptance (%)	1.6	1.0	1.0	2.0
Luminosity per IP ($10^{34}cm^{-2}s^{-1}$)	**5.0**	**16**	**115**	**0.5**

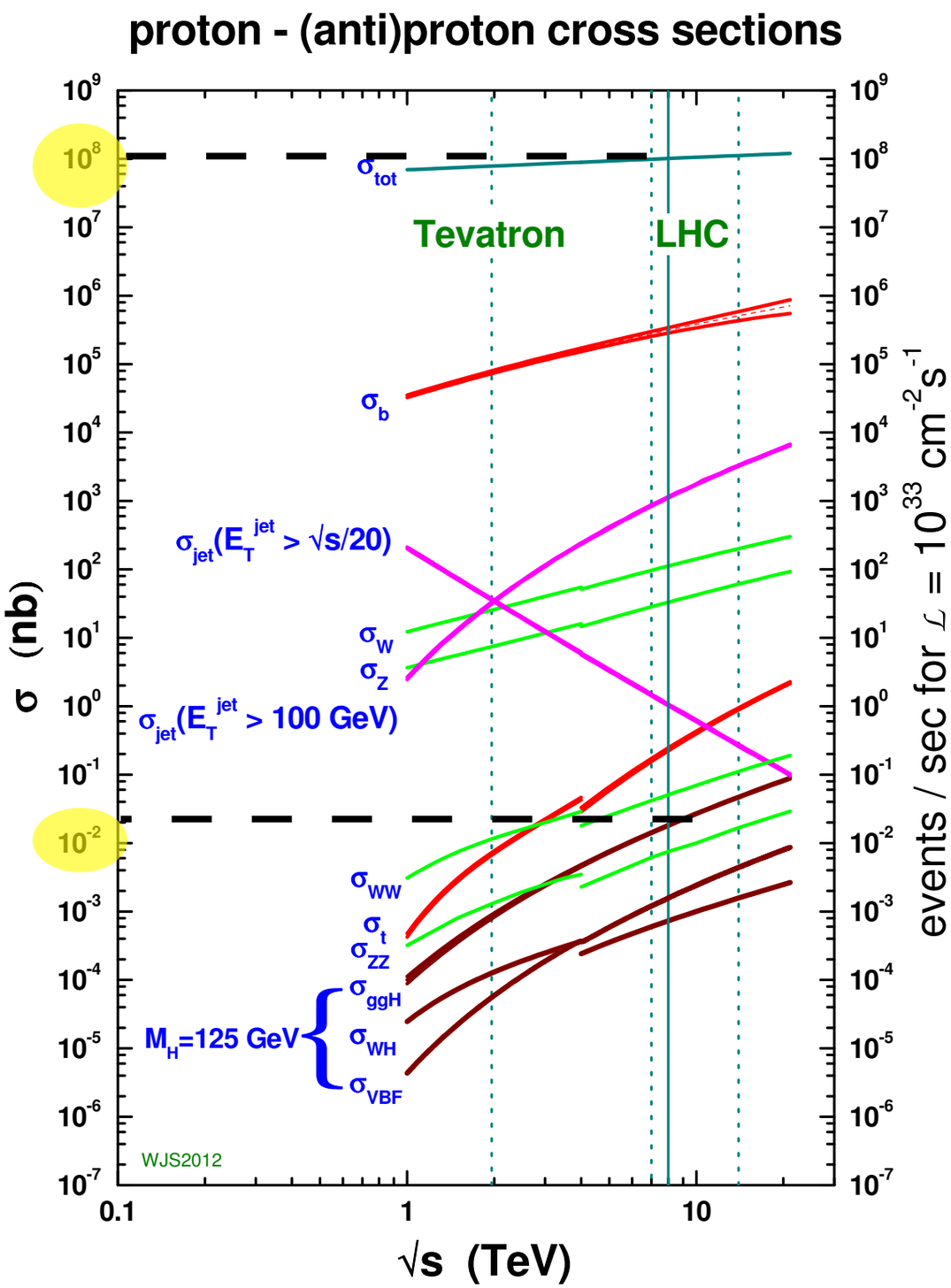
Key technology R&D in TDR phase

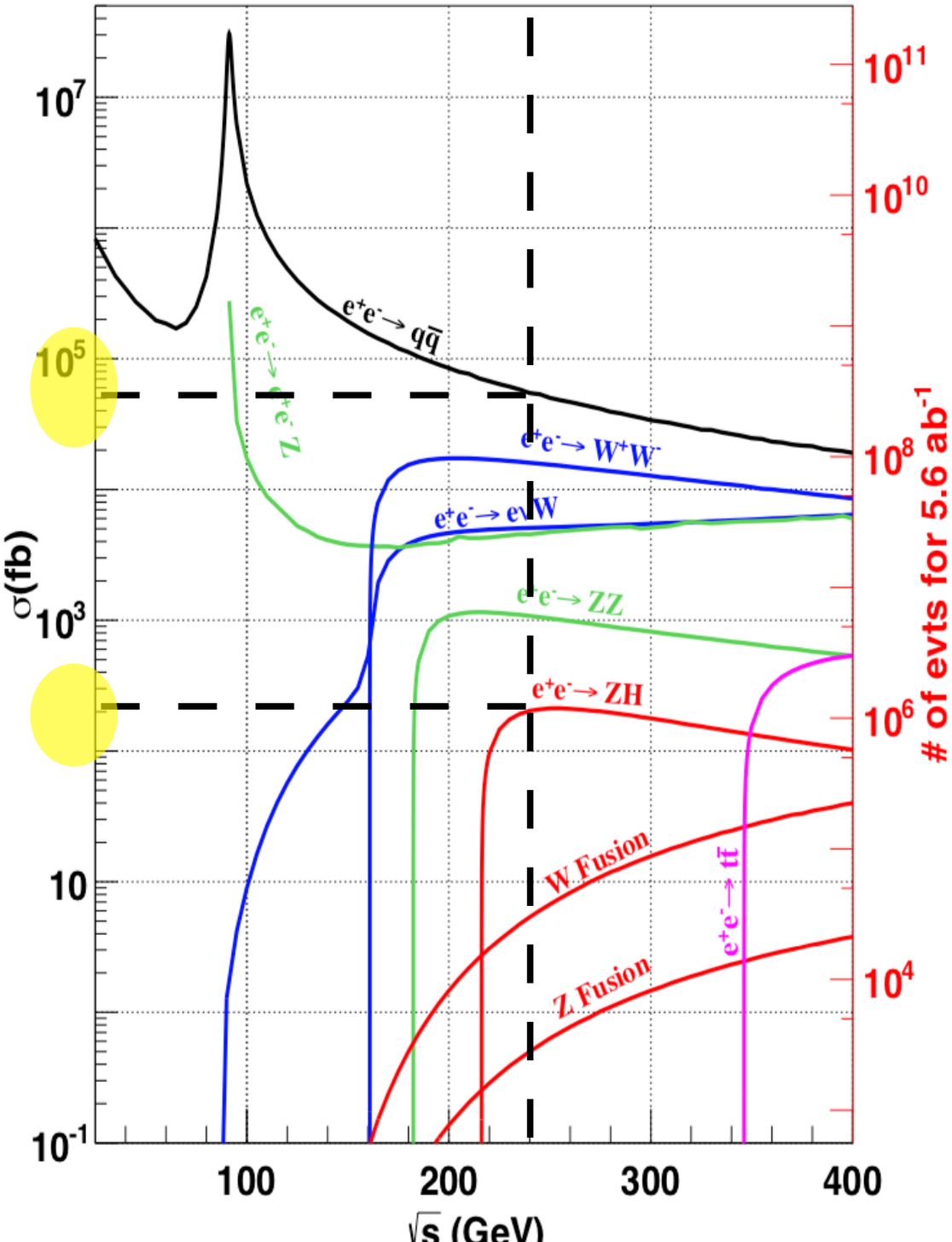
- **RF power supply and high efficiency klystron**
- **SRF cavities & modules (1.3G & 650MHz)**
- **Key components of the positron source**
- **High performance accelerator (S&C-band)**
- **Novel magnets: Weak field dipole, dual aperture magnets**
- **Injection/extraction**
- **Electrostatic deflector**
- **Vacuum chamber with NEG coating**
- **Instrumentation, Feedback system**
- **Cryogenic system**
- **Magnet power supply**

From: Jie Gao's accelerator talk in the CEPC Edinburgh workshop

SM backgrounds (pp vs ee)

- Backgrounds at pp colliders are typically >10 *orders higher* than signal





Overall requirement on detector

Detector requirements for high-energy e^+e^- colliders

Precision measurements

Require excellent **momentum resolution and flavor tagging**
- Low-mass vertex and tracking detectors, high granularity

Require excellent **energy resolution**
- Employ excellent calorimeters (particle flow, dual readout)

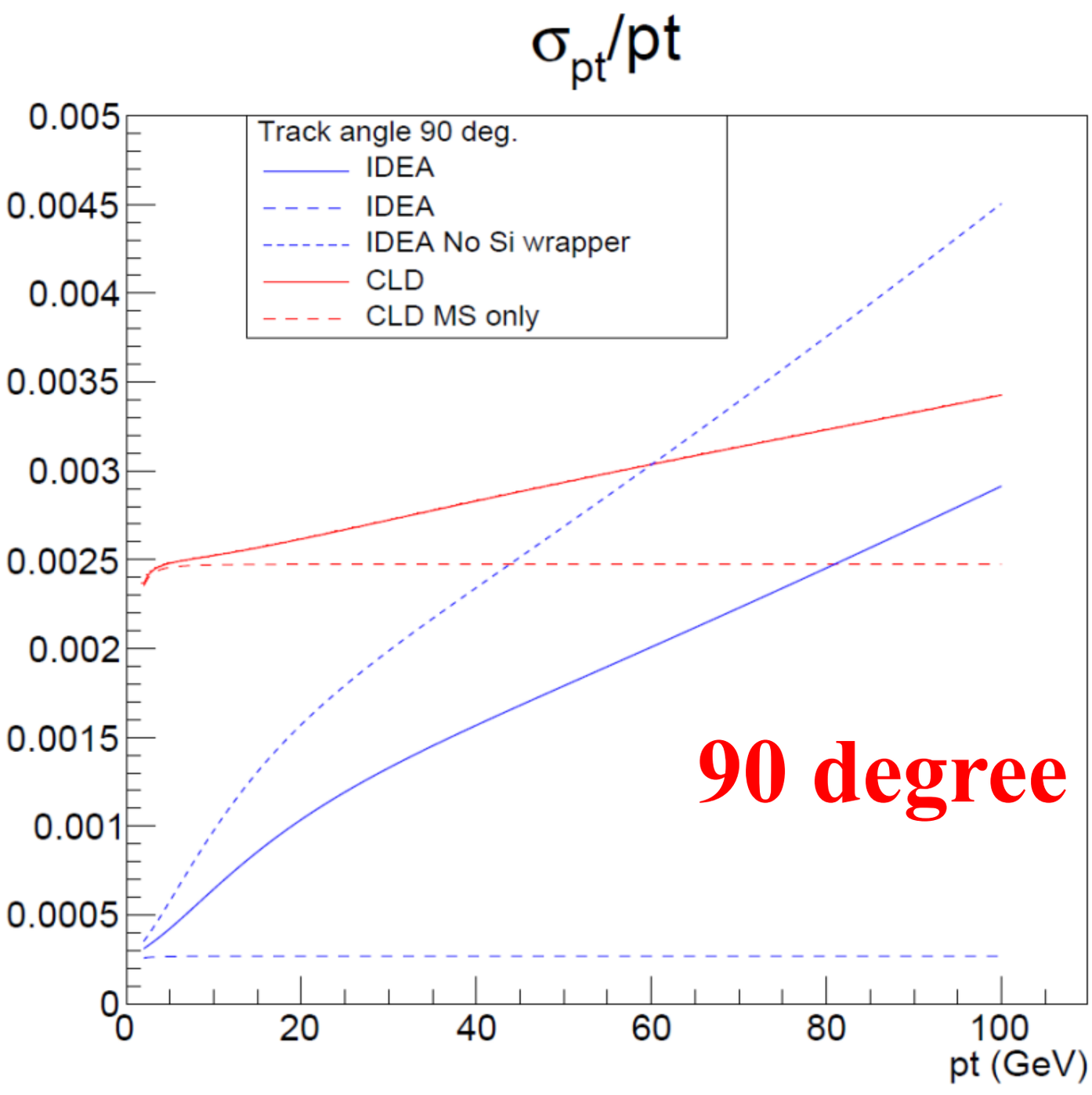
No major concerns about radiation hardness, unless for very forward detectors and inner most layer of vertex detector

Complementary subsystems

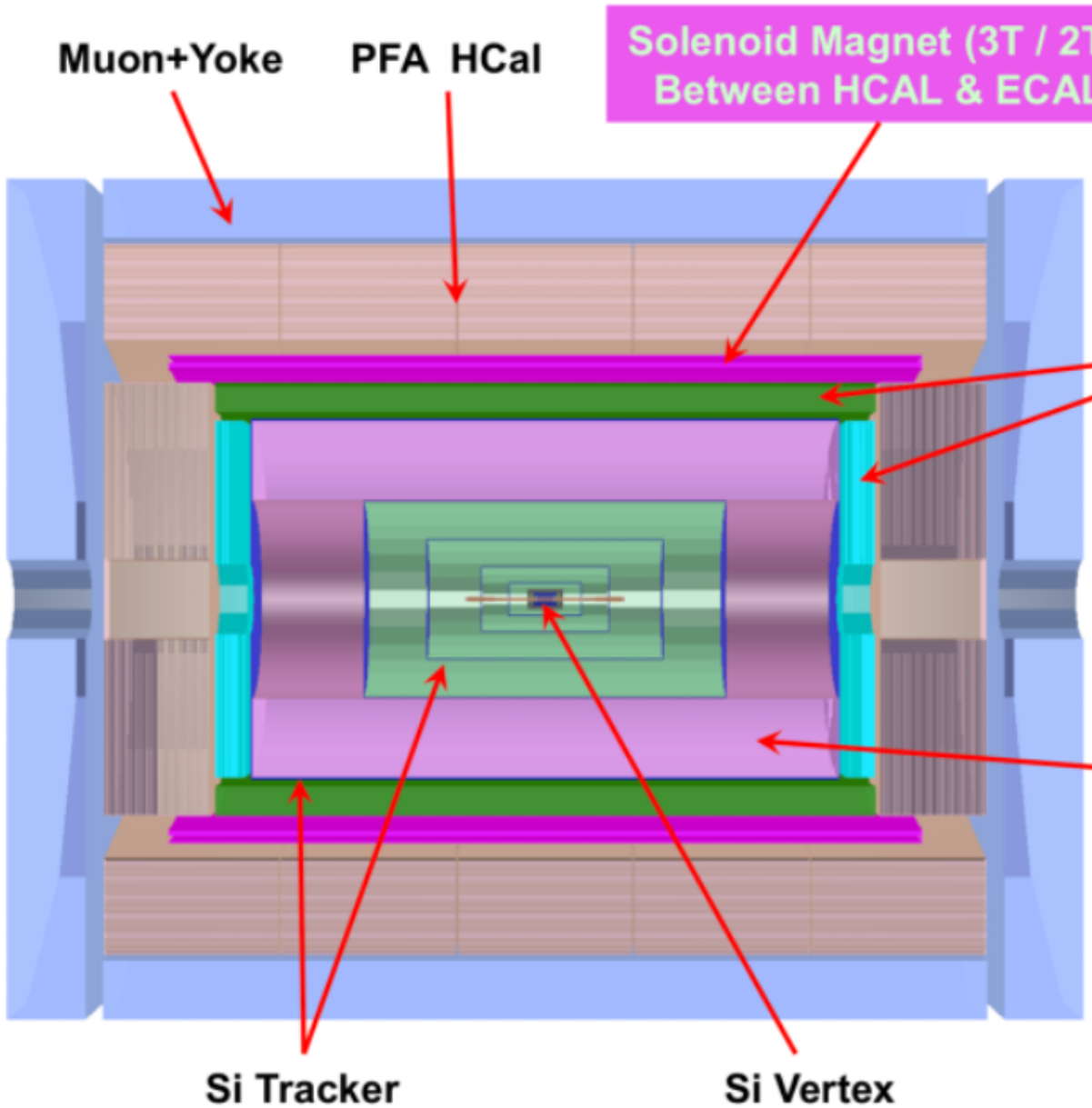
Subsystem	Measurement
Vertex detector	vertex position
	impact parameter → helps determine flavor
Tracking detector	track momenta of charged particles
ECAL: electromagnetic calorimeter	track momenta of charged particles
HCAL: hadronic calorimeter	energy of γ, $e^{\pm}$ and hadrons
Magnet system	energy of hadrons (including neutrals)
Muon system	bend charged particles → momentum measurement
Hermicity	identify muons
Luminosity detectors	missing energy (e.g. ν)
	luminosity

15

From João Guimarães Da Costa talk in CEPC workshop 2020


σ_{pt}/pt
Track angle 90 deg.
IDEA
IDEA
IDEA No Si wrapper
CLD
CLD MS only
0.005
0.0045
0.004
0.0035
0.003
0.0025
0.002
0.0015
0.001
0.0005
0
0
20
40
60
80
100
pt (GeV)
90 degree

Crystal Calorimeter based Proposal (2/3 T)



Advantage: the HCAL absorbers act as part of the magnet return yoke.

Challenges: thin enough not to affect the jet resolution (e.g. BMR); stability.

Transverse Crystal bar ECAL

Advantage: better π^0/γ reconstruction.

Challenges: minimum number of readout channels; compatible with PFA calorimeter; maintain good jet resolution.

Drift chamber that is optimized for PID

Advantage: Work at high luminosity Z runs

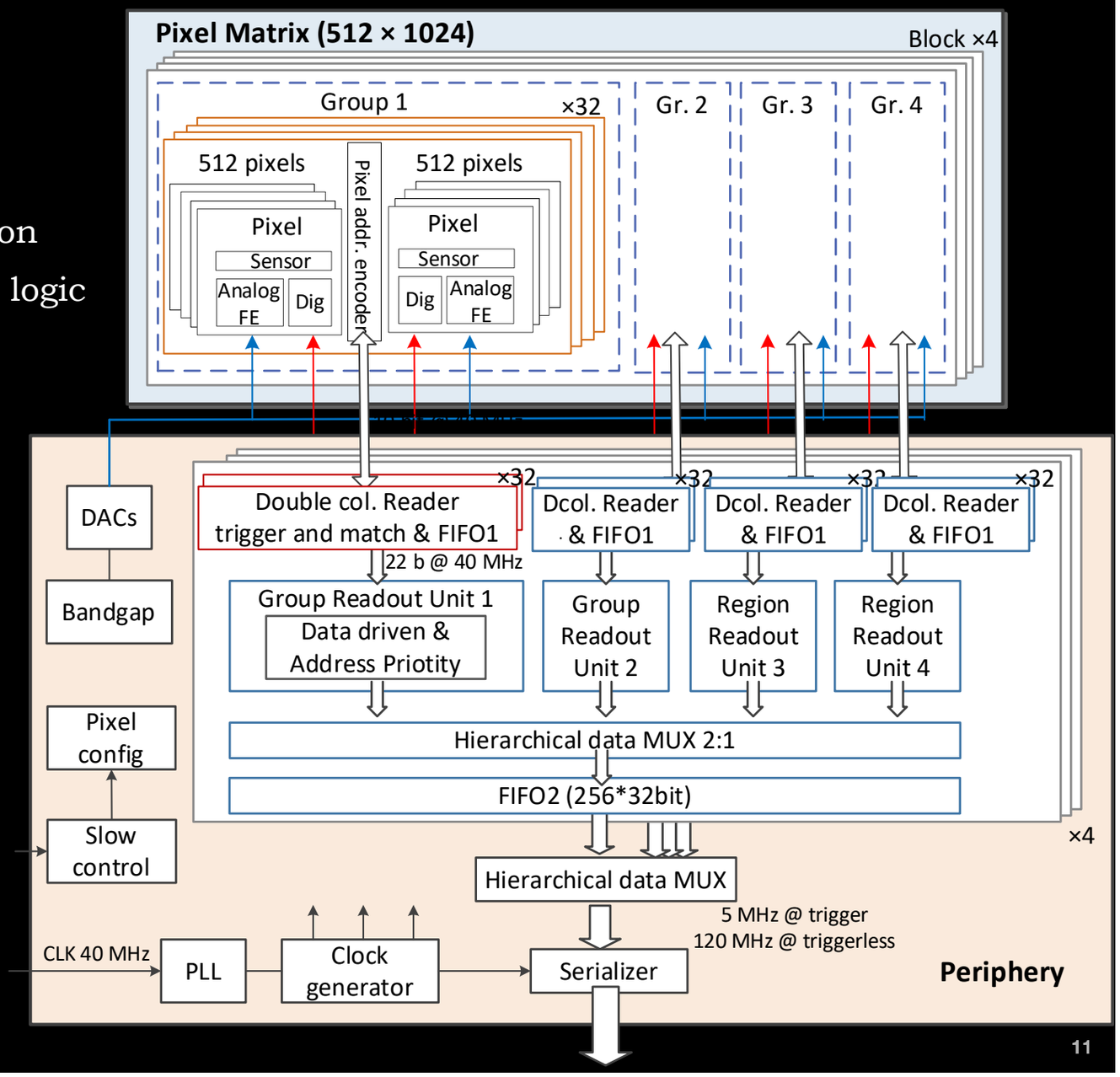
Challenges: sufficient PID power; thin enough not to affect the moment resolution.

TaichuPix readout

TaichuPix readout architecture

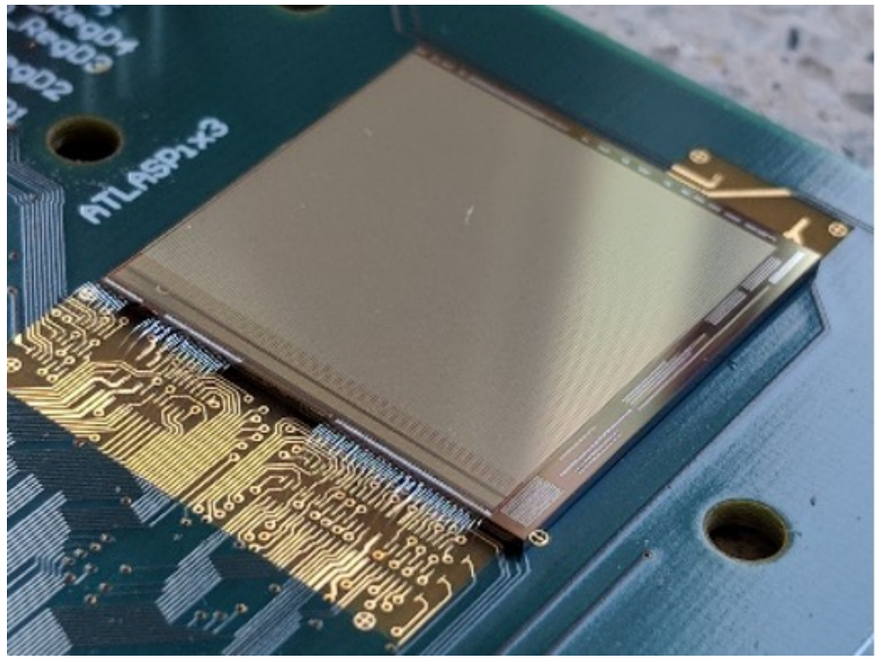
- **High resolution and high data rate**
- **Data-driven readout design**

- **Pixel 25 □m × 25 □m**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Readout time: 50 ns for each pixel
- **2-level FIFO architecture**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate
  - between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp
    only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.



ATLASPix3.1

- Originally developed for ATLAS
  - TSI 180nm processes
  - Excellent for HV-CMOS based system R&D
- Full reticle size of 2.2 cm x 2.0 cm
  - Features pixels of 50µm x 150µm
  - Matrix size 132 x 372
- Pixel readout
  - Pixels contain amplifiers and comparator with threshold tune circuit
  - Comparator is NMOS only
- Data output
  - 1.28 Gbit/s 64b/66b (triggered),or 1.6 Gbit/s 8b/10b (un-triggered)
- Clock data recovery from command in
- Shunt/LDO regulators for Serial Powering
- Power consumption 140 mW/cm2



I. Peric et al., High-Voltage CMOS Active Pixel Sensor, IEEE JSSC, Volume: 56, Issue: 8, Aug. 2021
https://ieeexplore.ieee.org/document/9373986

ATLAS Pix3.1

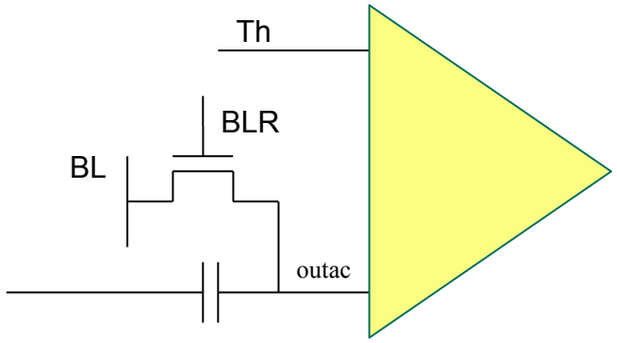
ATLASpix3.1

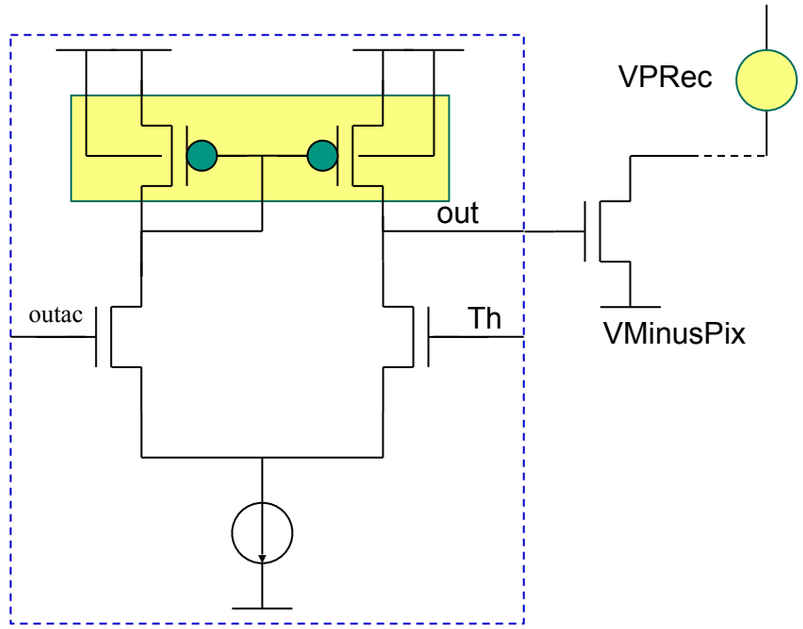
- ATLASpix3.1 submitted in December and delivered in February
- Redone masks for 8 Layers
- 12 wafers produced
- Reduced detector capacitance by replacing M2 shield with M3 shield (from about 250fF to 130fF)
- Modified design of the guard ring
  - Larger distance between DN and PW ring (see slides)
  - M1 ring disconnected from PW
  - Idea set substrate to -120V and M1 ring to -60V
- Added stability capacitor to the power regulator

Ivan Peric

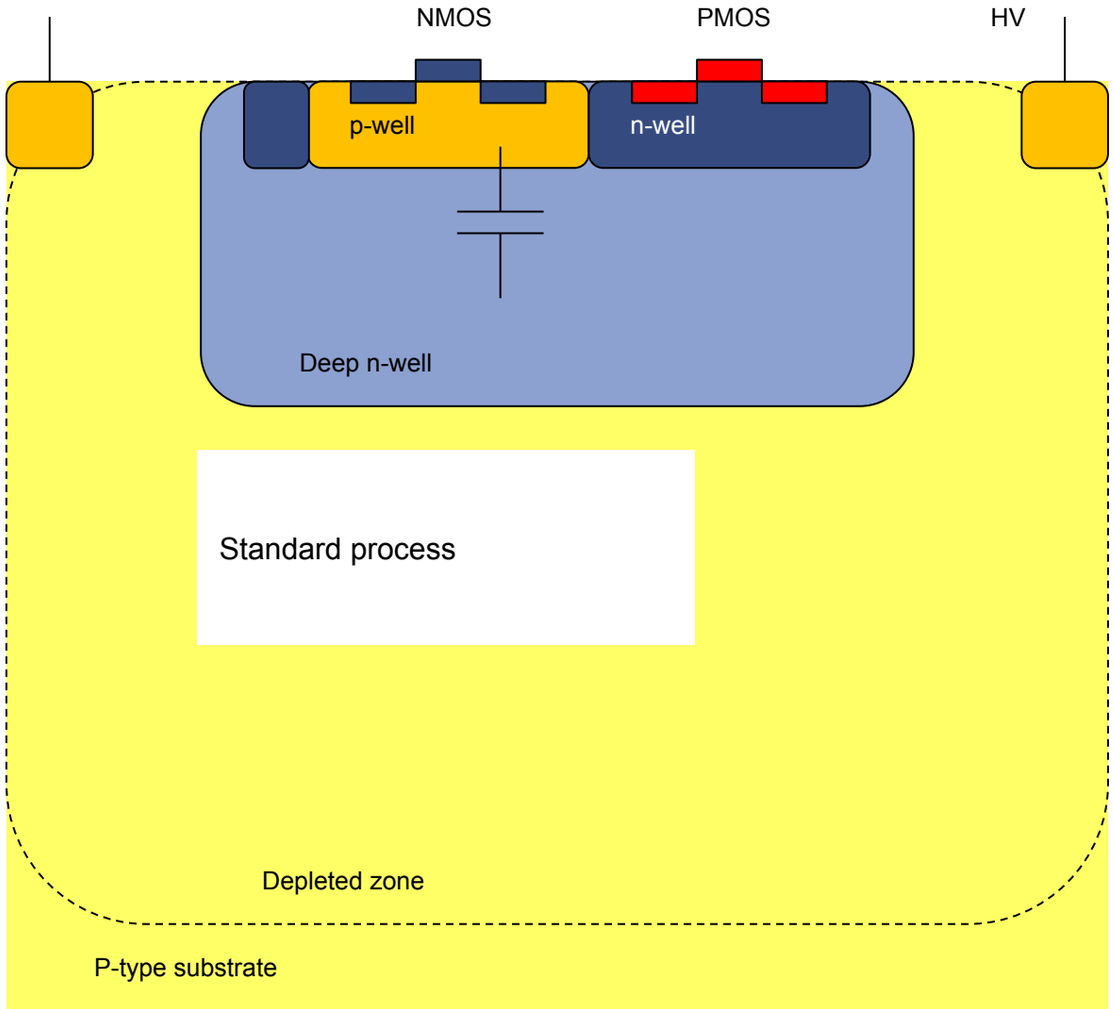
CMOS comparator

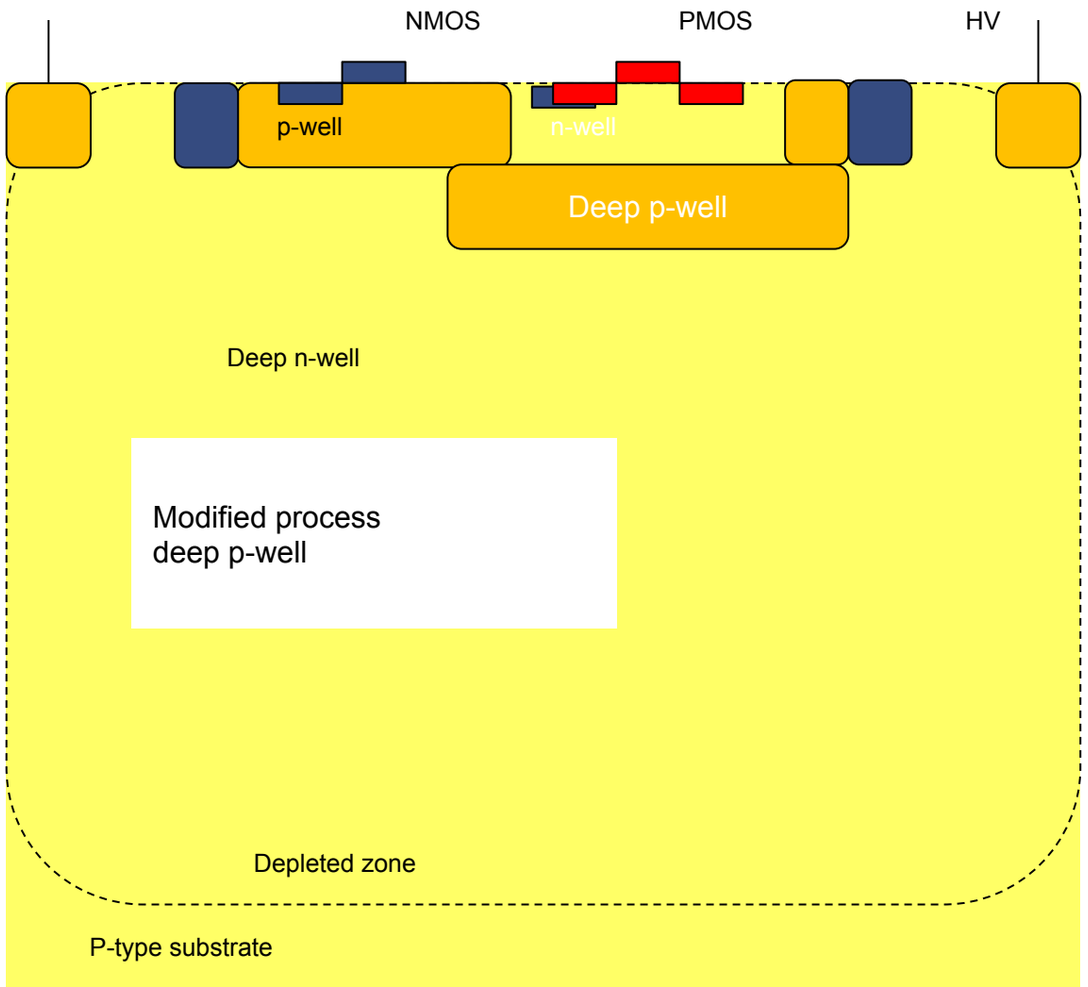
- Needs deep p-well
- Works with smaller bias current





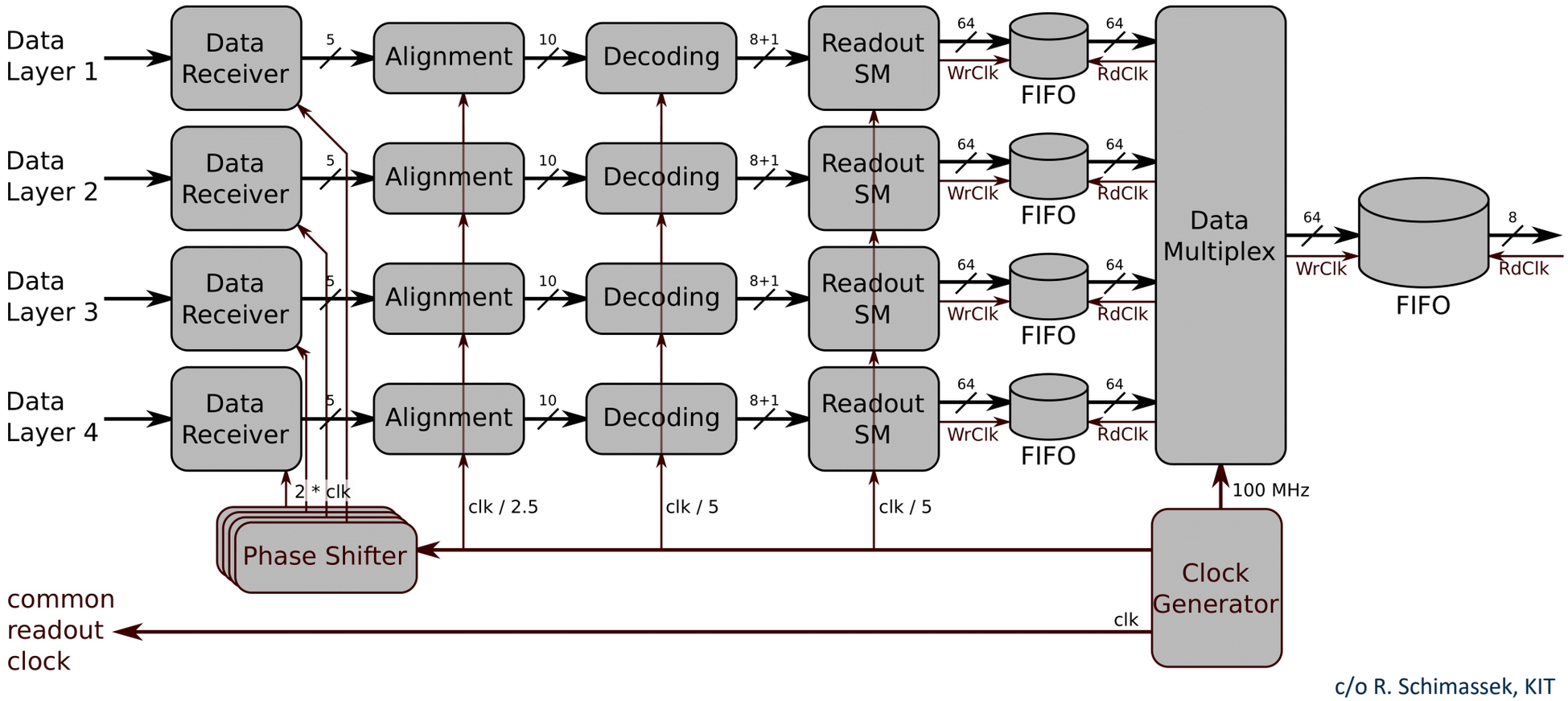
Ivan Peric: *UK-CEPC tracker workshop*





Firm-/Software changes for quad

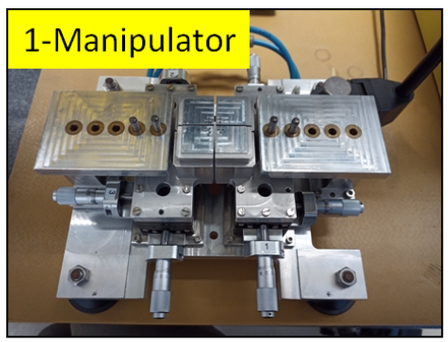
- Firmware:
  - Multiplication of the **elemental structure** for the single chip
- Software:
  - Configuration with SPI and CMD
  - Chips can be configured **simultaneously** or **individually**

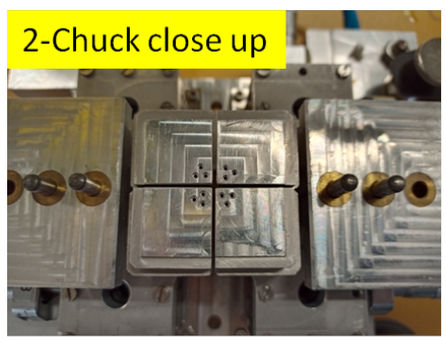


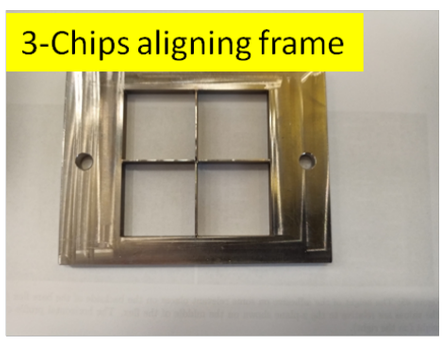
c/o R. Schimassek, KIT

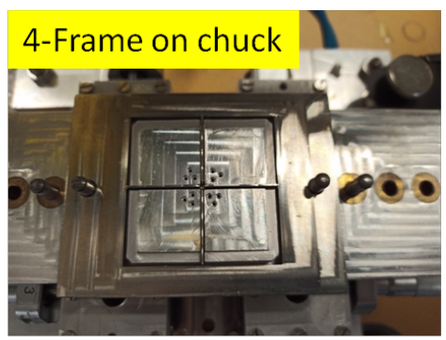
Assembly procedure

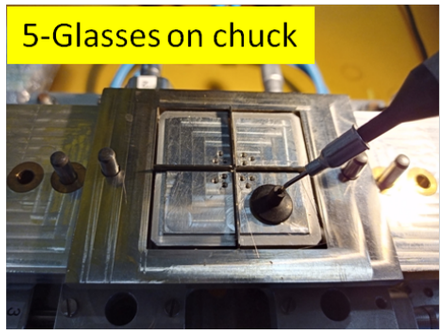
- Shown with **glass squares**: same procedure also used for real module assembly
- Gap between chip of **100 um ± 50 um** has been achieved

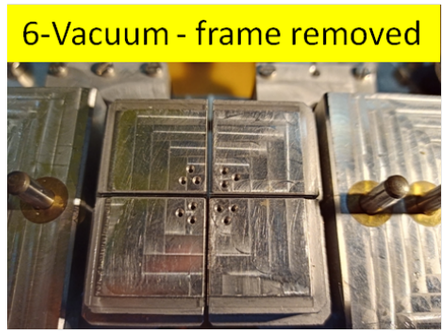


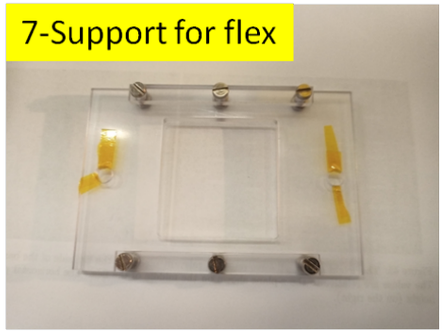


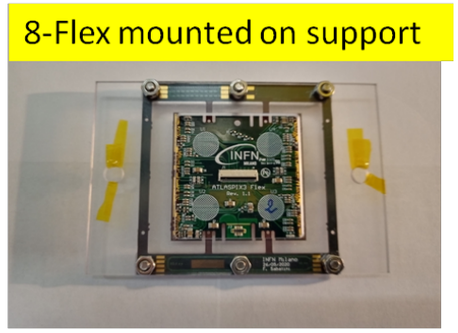


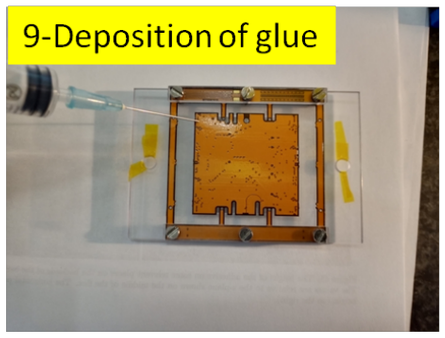


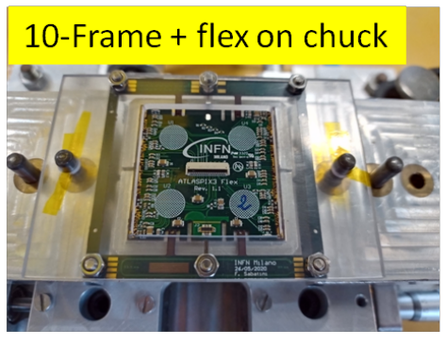


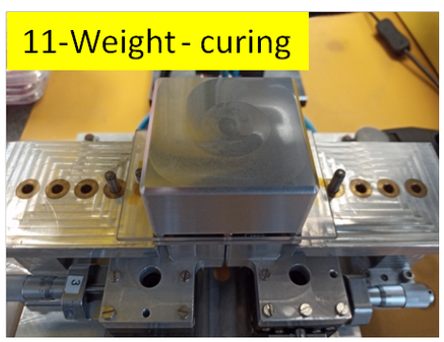


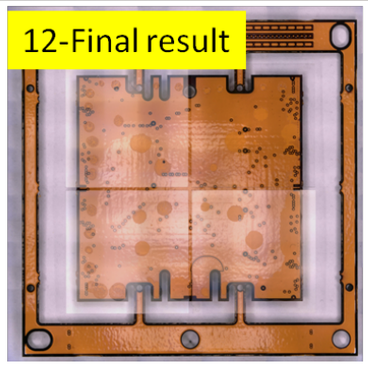












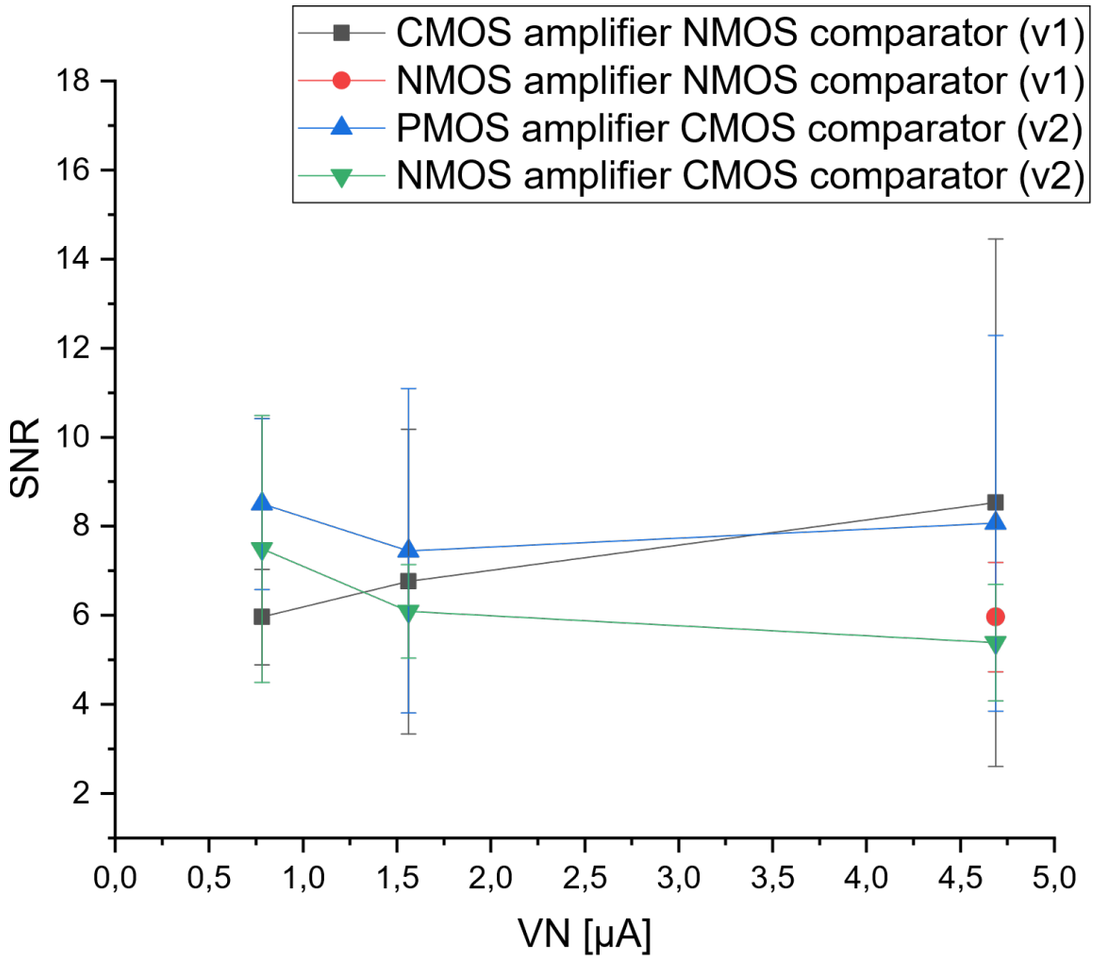
Improvements for sensors beyond ATLASPix3

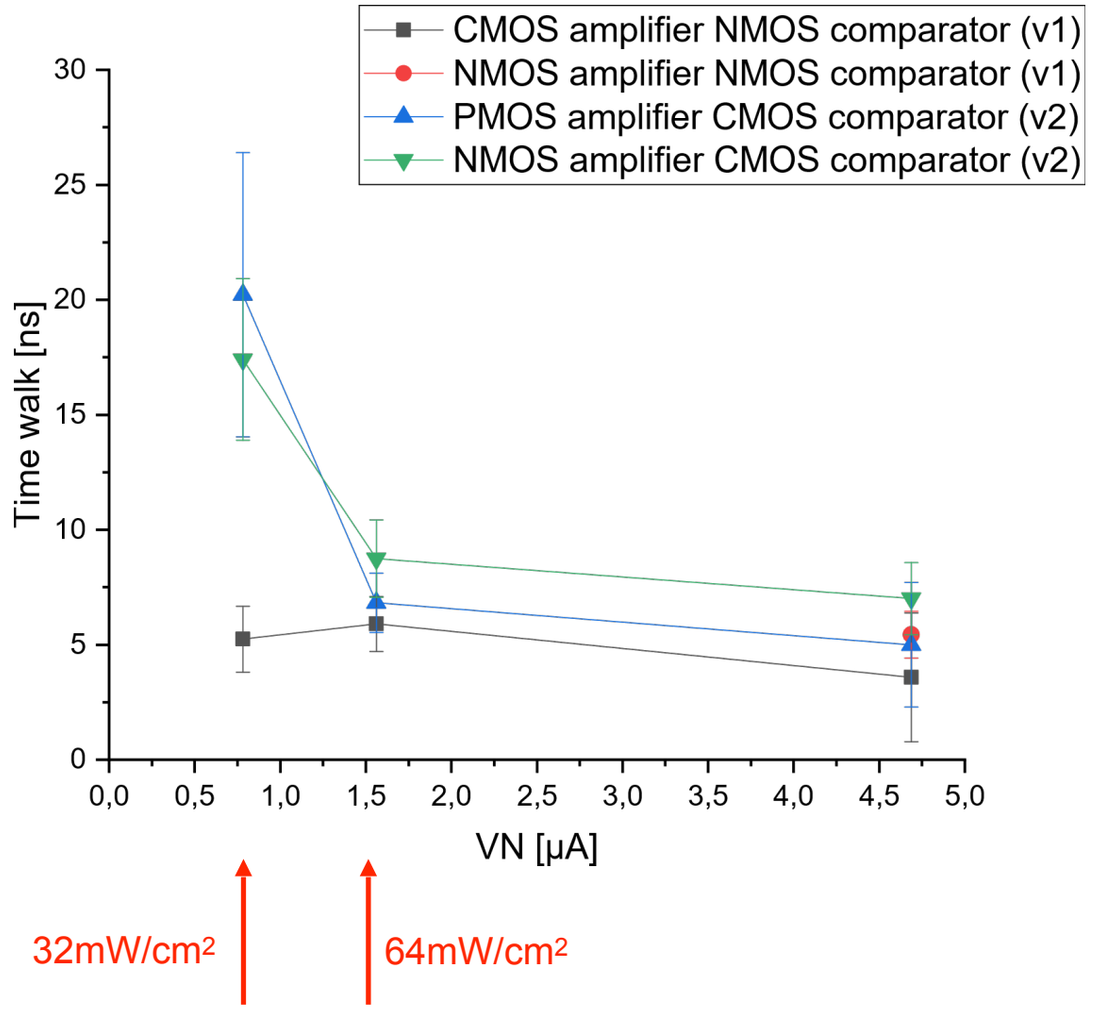
Ivan Peric

- Options:
  - Different pixel sizes
  - Different amplifier types (NMOS and PMOS)
  - Different comparator types (NMOS, CMOS and distributed)
  - Different TDAC types (placed in pixels or in periphery)
- Fixed improvements versus ATLASPIX3
  - Hit buffer cell with time to digital converter (supports time resolution ~ 100ps), TDAC, differential receiver for distributed comparator
  - Possibility of daisy-chain readout – one chip acts as data collector for another
  - Possibility to bias pixel n-well with voltage higher than 1.8V, and to bias pixel p-well with voltage lower than 0. It reduces capacitance. Reduced capacitance means better time resolution for the same power consumption.
- PMOS amplifier has lower noise than the NMOS amplifier when the bias current is high (~10µA). It has better (smaller) time walk for threshold of nine sigma noise. PMOS amplifier is more suitable for larger pixels i.e. pixels with larger capacitance (larger than 150fF)
- NMOS amplifier has better time walk for nine sigma noise for small bias currents (~1µA). It is a good choice for small pixels with little capacitance. Some risk because NMOS has more flicker noise and because we have little experience with this amplifier type
- NMOS comparator is the standard comparator type we used so far. It has some disadvantages: rather high current consumption (~3µA), larger delay than CMOS comparator, need for additional bias voltage of 2.1V, output signal of reduced amplitude, it occupies large area and causes large detector capacitance
- CMOS comparator does not have the disadvantages of NMOS comparator, it is faster for the same current consumption, potentially more radiation tolerant, smaller. Disadvantage is that CMOS comparator needs additional deep p-well implant (iso-PMOS option). This implant will be produced by TSI for the first time – there is some risk that it does not work.
- Distributed comparator has only three transistors in the pixel and adds very little capacitive load. The receiver and TDAC are placed in the hit buffer at the periphery. It is fast, low power and does not require additional iso-PMOS. The disadvantage is that it requires two lines per pixel to connect it with the hit buffer. This is not a problem for pixels larger than 50µm x 150µm.
- TDAC can be placed in pixel but it adds detector capacitance. TDAC can also be placed at the periphery, in this case it makes periphery slightly larger

Preliminary measurements and implications

- Pixel matrices with three amplifier types have been operated with smallest possible threshold
- Signal to noise ratio (from ToT) and time walk for signals larger than 3200e have been measured
- CMOS amplifier has smallest time walk
- **Low power consumption is possible (up to factor of 4 reduction compared with ATLASPix3)**





ATLASPIX3: 140mW/cm²

Link to Ivan Peric's talk at the UK-CEPC tracker workshop Nov 2021

55nm HV-CMOS development - HLMC

上海华力微电子有限公司
Shanghai Huali Microelectronics Corporation

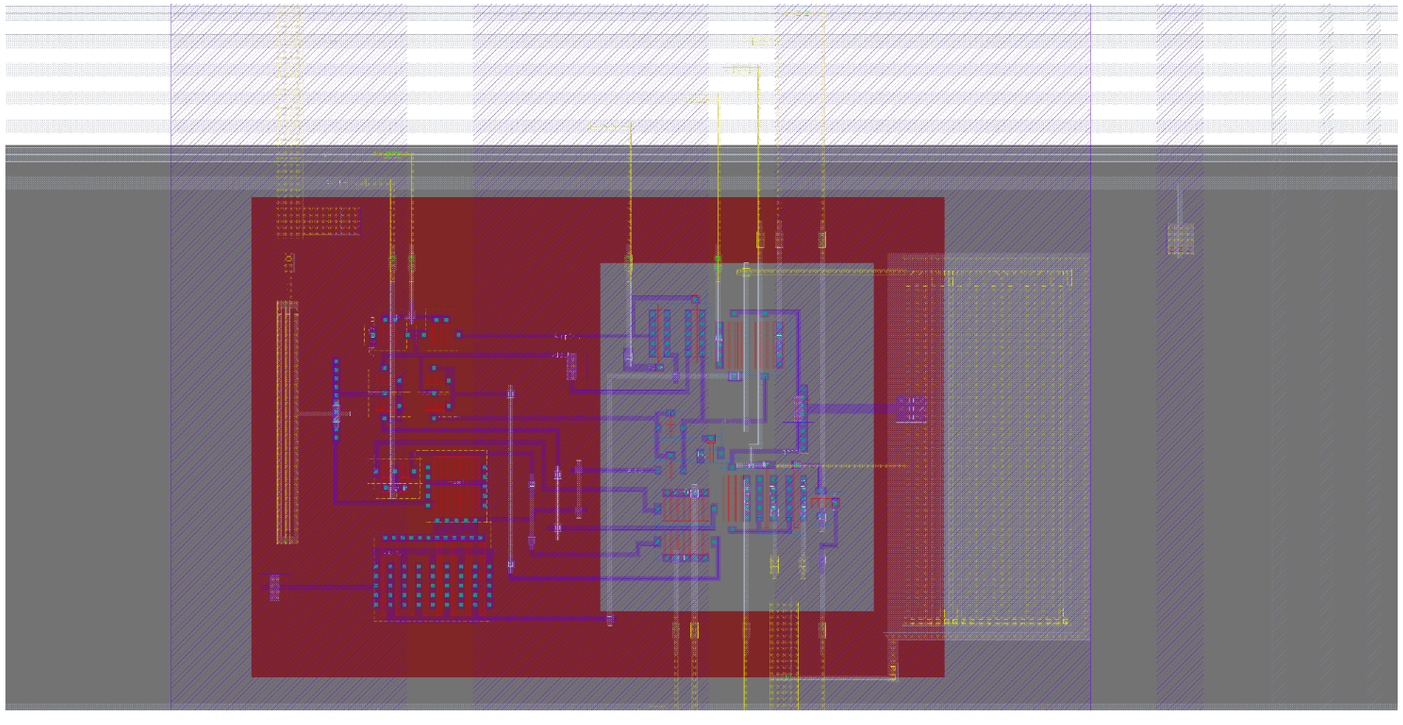
Shanghai Huali Microelectronics Corporation (**HLMC**) is a Chinese foundry. As of 2018, HLMC had 55 nm, 40 nm, and 28 nm process technologies and are capable of producing up to 35,000 wafers per month.

- HLMC technology offers similar layers as TSI
- Especially important is the floating logic structure with deep n-well
- The maximum voltage for HV transistors is 32V
- Deep n-well to p-substrate should have higher breakdown
- Metal layers 1 – 6 can be used for fine pitch routing
- The realistic pitch is down to 0.2um – relaxed and according to recommendation is 0.3 (in 180nm was 0.6)
- There are tree more thick metal layers, suitable for power
- Low voltage power supply is 1.2V
- There are only hspice models available, we used Mentor Calibre for DRC LVS

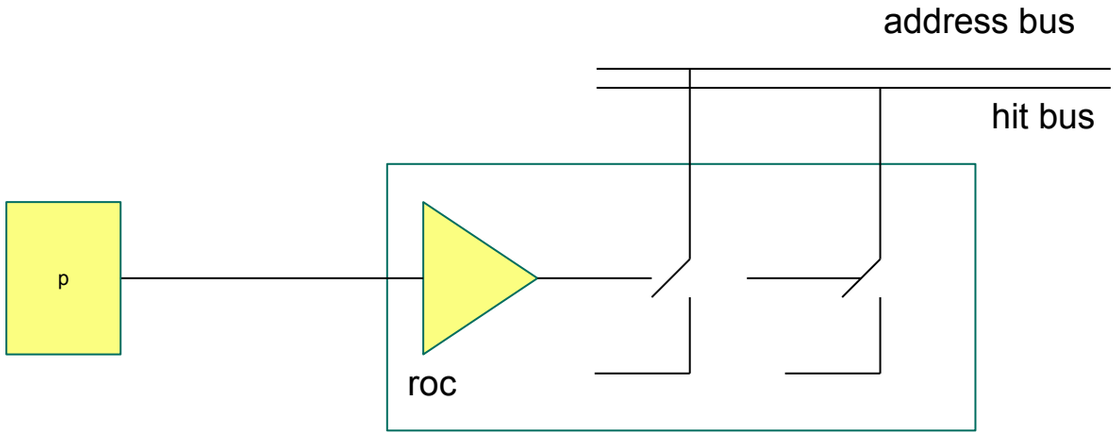
Link to Ivan Peric's talk at the UK-CEPC tracker workshop Nov 2021

HV-CMOS sensor in 55nm technology (II)

- The pixel size is **x = 252 µm, y = 22 µm** (smaller x dimension is possible)
- The pixel contains CSA, CR filter and differential output driver
- Every pixel has a readout cell placed at the periphery
- One readout cell contains differential receiver – the driver (in pixel) and the receiver form a distributed comparator
- The structure of readout cell is simple, the comparator output is connected to hit bus driver and to address ROM. The ROM cells pass the data to the 10 bit address bus
- The readout cell also contains two bit-register to store comparator enable and injection enable bits
- The size of the readout cell is 4.2µm x 60µm (relaxed layout)



Pixel layout

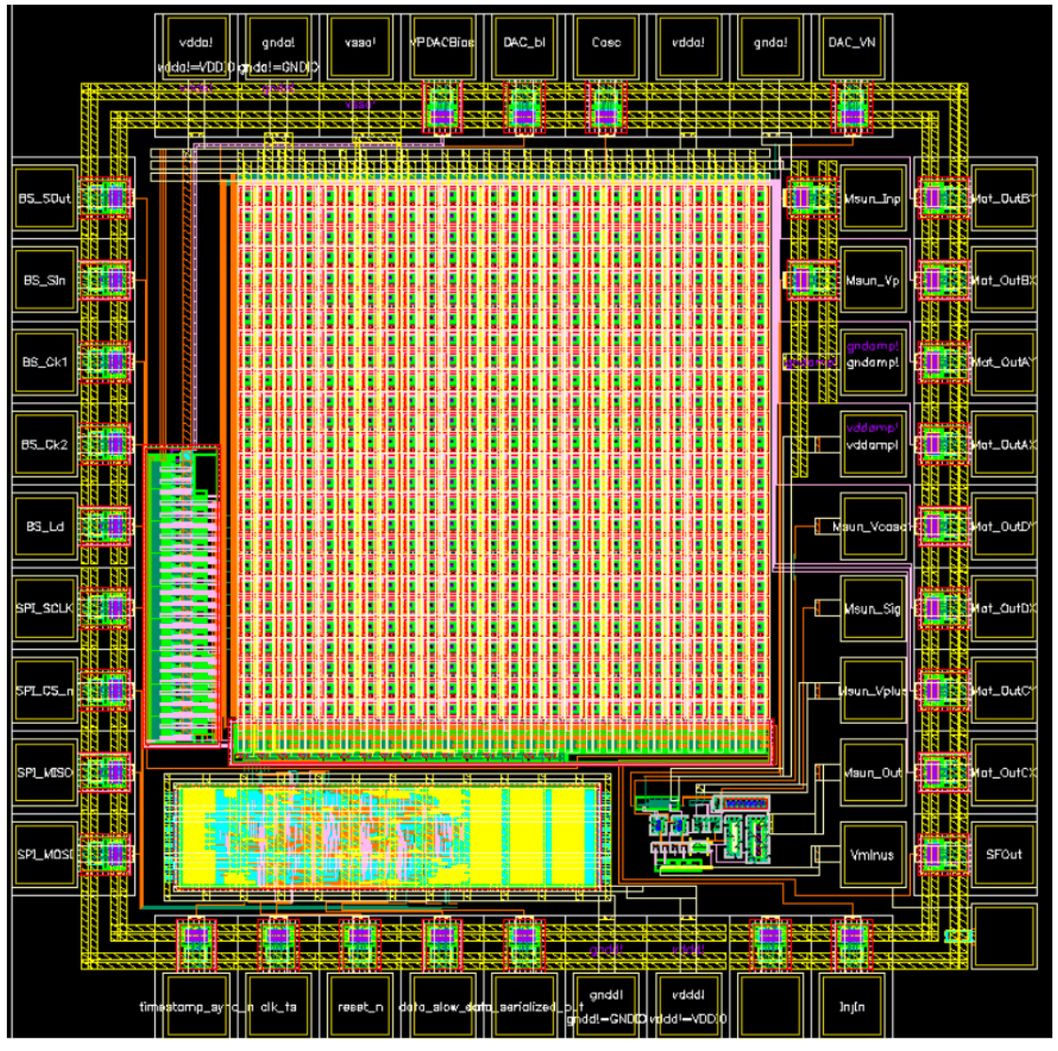


pixel p and readout cell

55nm HVCMOS - CEPCPix1 at SMIC

中芯国际集成电路制造有限公司
Semiconductor Manufacturing International Corporation

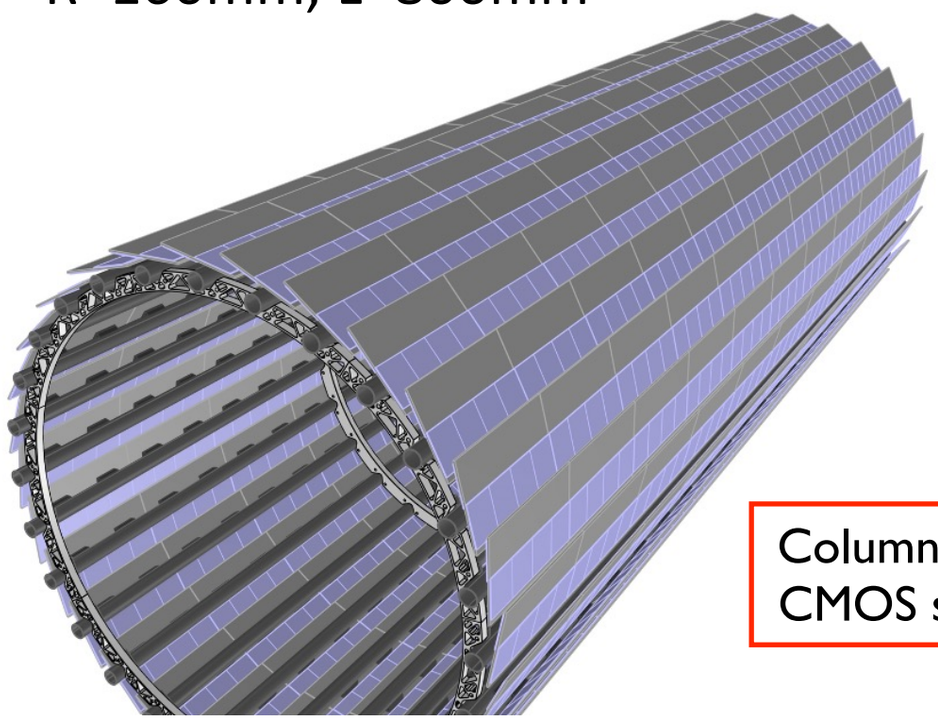
- Timestamp measurement:
  - Two columns use digital encoding of pixel address and 24 columns use analog encoding of addresses
  - leading & trailing edge timestamp
  - Address double check for hit consistency
- Digital Readout FSM:
  - Polling readout of 4 hit channels
  - Compatible with test mode
- Digital Interface
  - Synchronous serialized slow output
  - Asynchronous serializer
  - SPI configuration

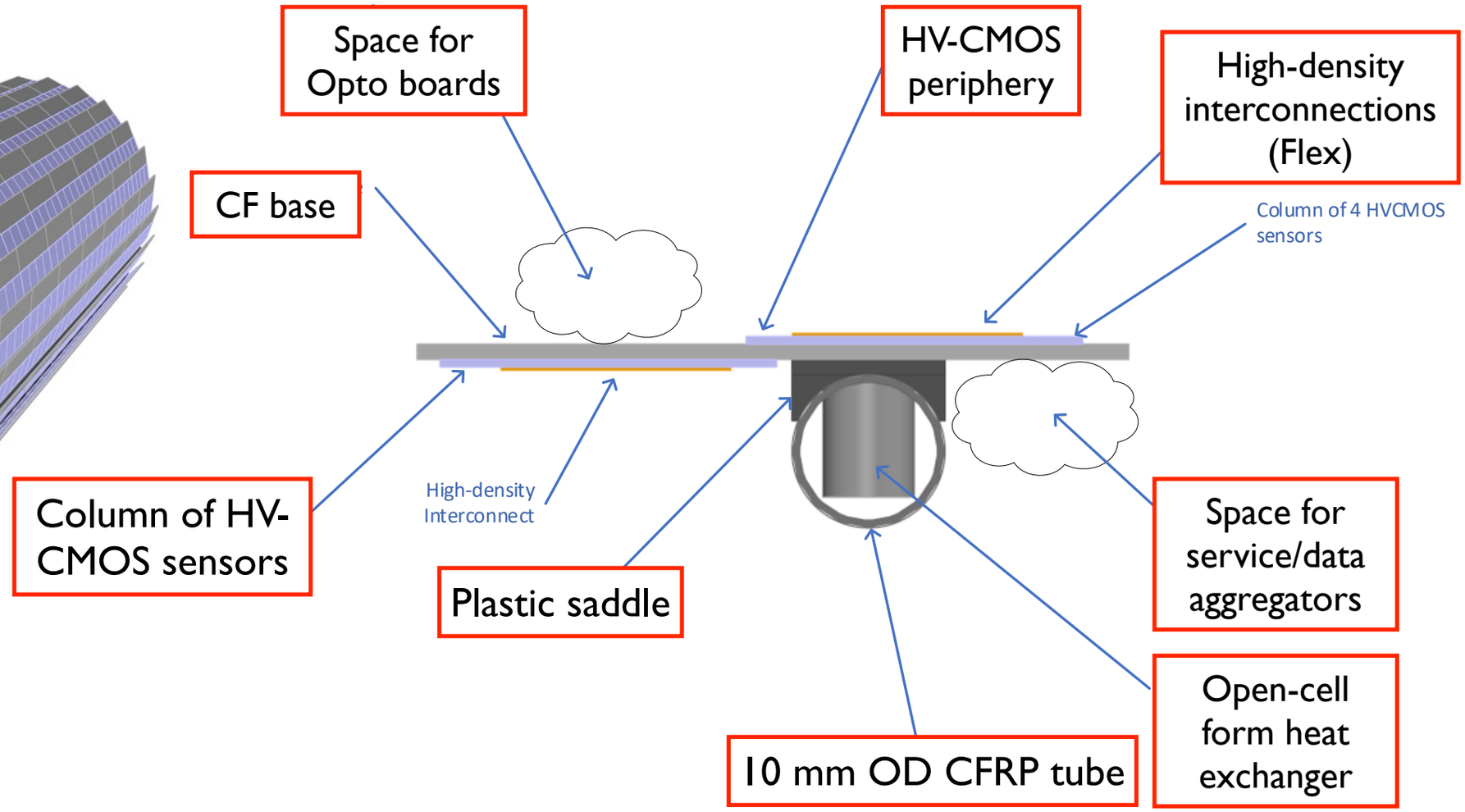


Talk by Hui Zhang (KIT) in CEPC 2023 Workshop in Nanjing

Mechanical design concept for SIT-1

R=160mm, L=800mm





- HV-CMOS sensors glued to CF base
  - Asymmetric arrangement with peripheral areas as close as possible to the middle where power consumption is max
- Base attaches to support tube via two saddles
- Saddles have apertures through which the foam heat exchangers pass and glue to the base