UNIVERSITÄT BONN

SI LAB
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CHRISTIAN BESPIN

BONN CMOS R&D

AN OVERVIEW OF 10 YEARS OF MONOLITHIC CMOS DEVELOPMENT

CURRENT AND FUTURE TRACKING AND VERTEXING DETECTORS 2023
QUEEN MARY UNIVERSITY OF LONDON

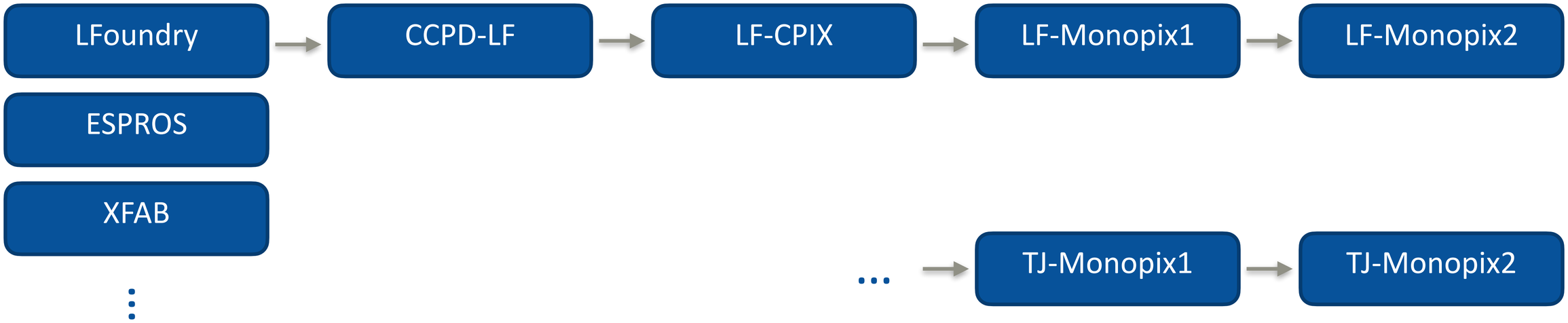
OUTLINE

- Early developments (ESPROS/Toshiba/XFAB/CCPD_LF)
- Towards larger demonstrators and fully monolithic (LF-CPIX, LF-Monopix1, TJ-Monopix1)
- Excursion: passive commercial CMOS sensors
- Current prototypes (LF-Monopix2, TJ-Monopix2)
- Bonn as R&D site

This talk is an overview of many years of developments with more people involved than I can mention. Most of the design and measurement efforts are achieved within collaborations.
For all the presented chips, only a selection of results is shown. Where available, I put references to publications with more detail.

CMOS DEVELOPMENT OVERVIEW

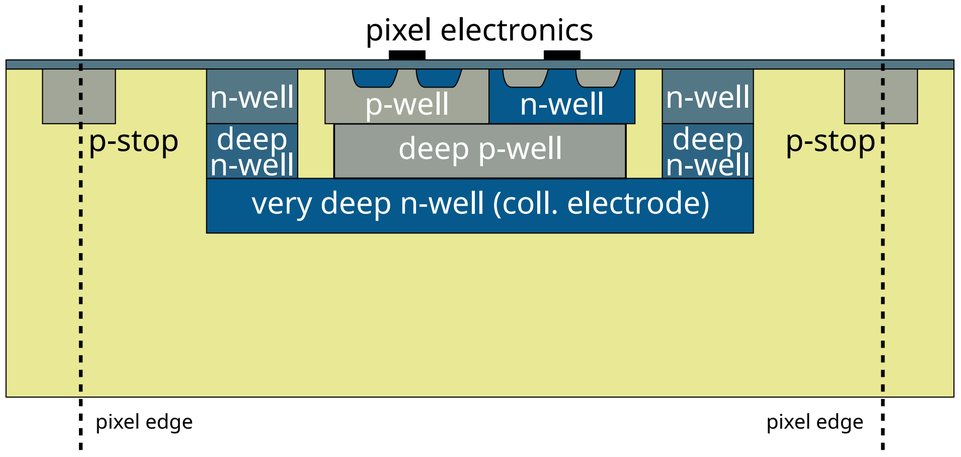
- Started beginning of 2010s with multiple foundries: XFAB, ESPROS, Toshiba, LFoundry (to name a few)
- Simpler prototypes evolved into larger ones, sticking with (mainly) LFoundry technology
- Two fully monolithic large-scale chips in 2017
- Second iteration of both Monopix chips received in 2021, ongoing characterisation



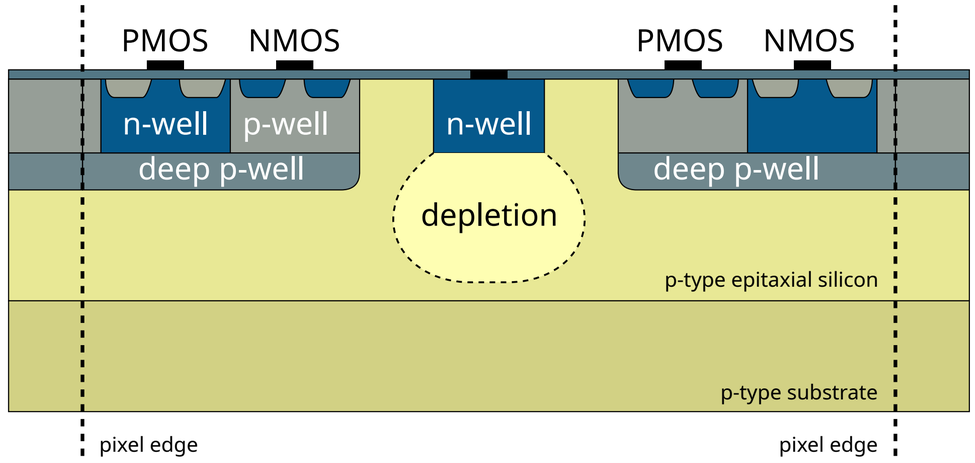
DEPLETED MONOLITHIC ACTIVE PIXELS

- Originally developed for ATLAS ITk outer layer requirements
- MAPS in commercial CMOS processes viable, but need depletion for speed and radiation hardness
- Use high voltage and/or high resistivity silicon technology ($d \propto \sqrt{\rho V}$)
- Two approaches: large and small collection electrode with integrated and separated readout electronics, respectively

Large collection electrode



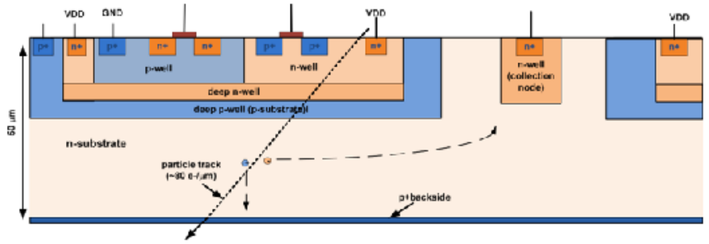
Small collection electrode



ESPROS / XFAB / TOSHIBA PROTOTYPES

EPCB01 & EPCB02

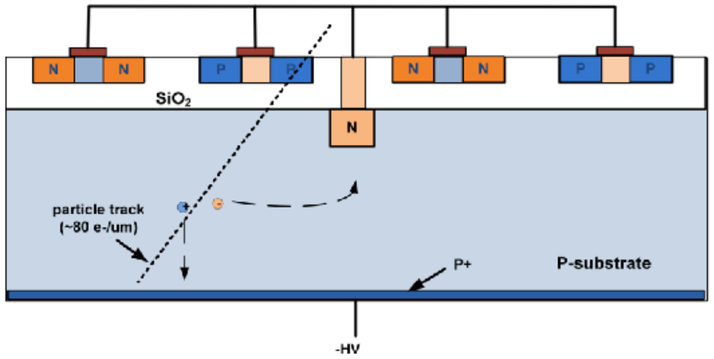
- ESPROS 150 nm CMOS



- 40 x 40 µm pixel size
- Small collec. electrode
- Binary digital readout

XTB01

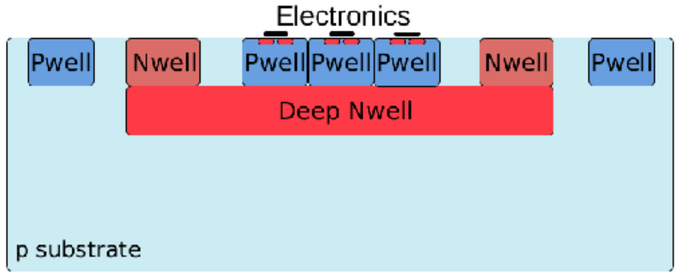
- XFAB 180 nm HV-SOI



- 25 and 50 µm pixel pitch
- Small collec. electrode
- Analogue signal only

TSB01A

- Toshiba 130 nm CMOS



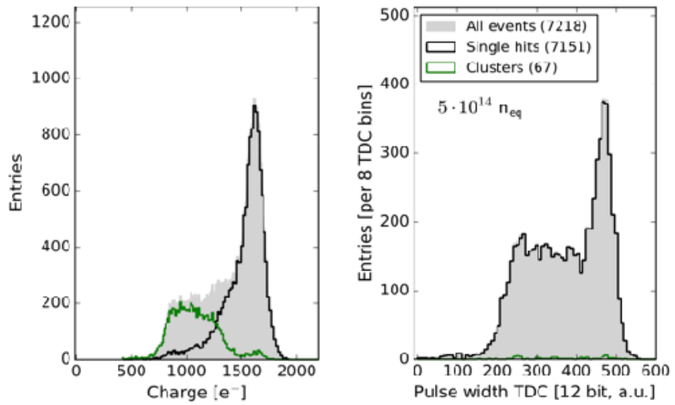
- 20 and 40 µm pixel pitch
- Large collec. electrode
- Analogue rolling shutter

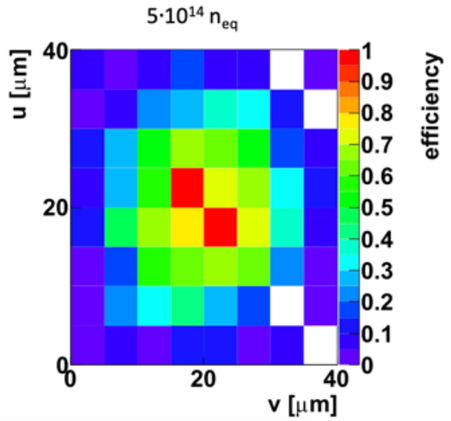
doi.org/10.1088/1748-0221/10/03/C03049

doi.org/10.1016/j.nima.2015.02.066

ESPROS / XFAB / TOSHIBA PROTOTYPES

EPCB01 & EPCB02





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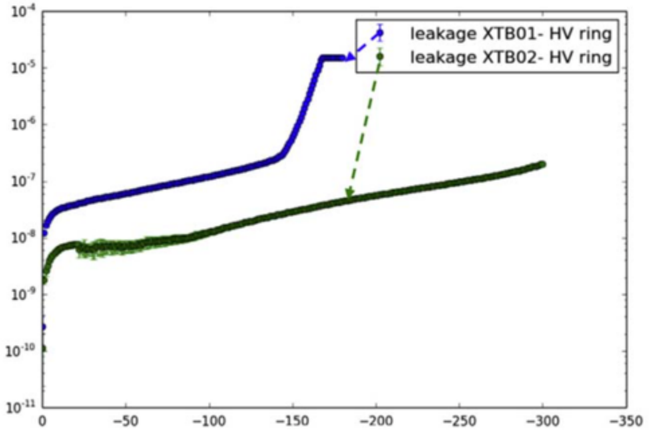
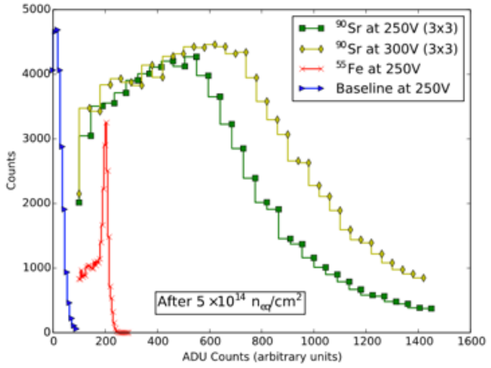
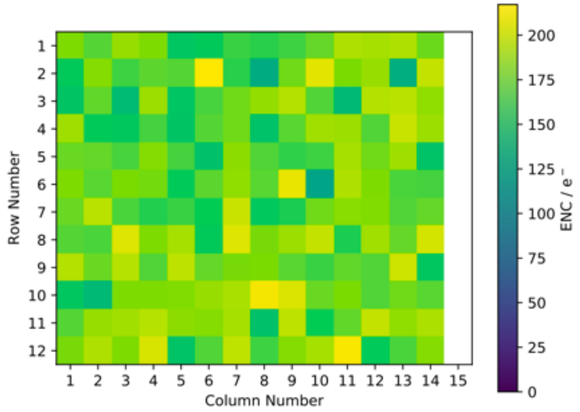
XTB01

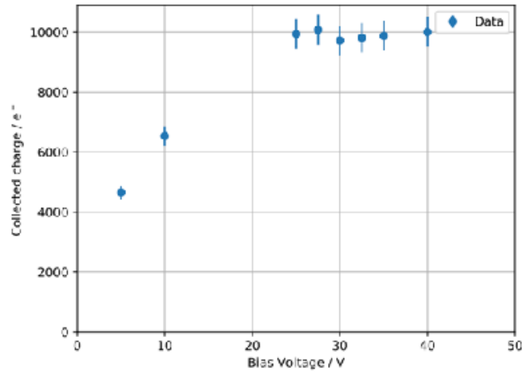




doi.org/10.1016/j.nima.2015.02.066

TSB01A





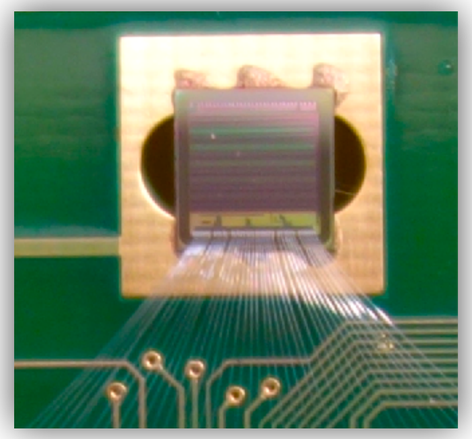
INTERLUDE

- This is only a selection of initial prototypes, of which none made it to a demonstrator stage
- Reasons were not only of physics nature
- In the following, focus on LFoundry development from prototype to fully monolithic detector
- Design is driven by cooperation of
  - University of Bonn
  - CPPM Marseille
  - IRFU CEA Saclay
  - (KIT, Karlsruhe – only CCPD_LF)

- In a later stage, TowerSemi developments emerged in cooperation with CERN (later in this talk)

CCPD-LF (2014)

- DMAPS implemented on highly resistive wafer in LFoundry 150 nm CMOS technology
- Main purpose: evaluate sensing and analogue front-end performance
- Hard facts:
  - Ca. 5 mm x 5 mm matrix size with 33.3 µm x 125 µm pixels
  - Two sensor types and three analogue front-end variants (CSA)
  - 4-bit local threshold adjustment (TDAC) in each pixel

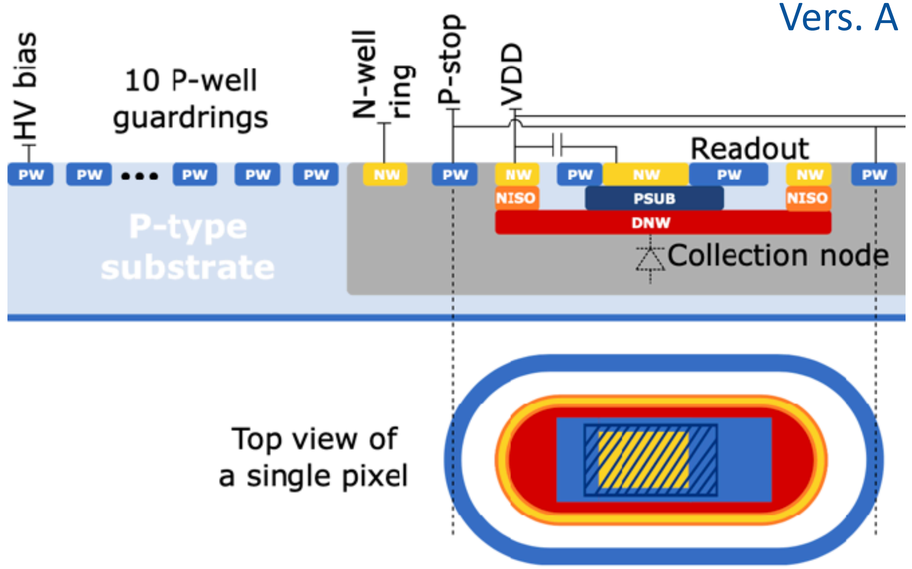


- Analogue output or binary readout, the latter with slow shift register (monolithic), or capacitively coupled to FE-I4 (hybrid, from ATLAS IBL)

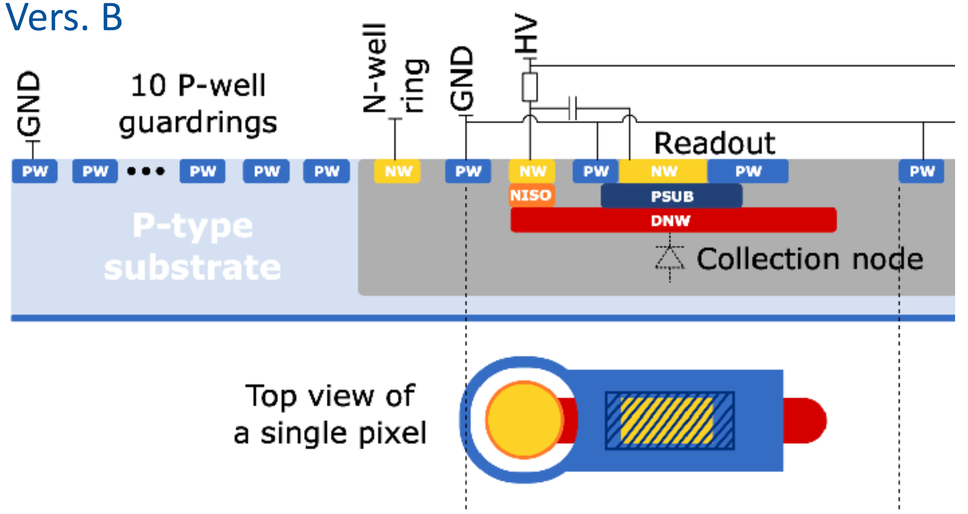
CCPD-LF (2014)

- Sensor geometry with large collection electrode (front-end electronics covered by n-well) or „small“ collection electrode (actual size is similar, but is close to a true small-electrode design)
- In the former, negative bias is applied on the substrate, limited by diode breakdown
- In the latter, AC coupling of signal, positive bias on collection well, limited by AC capacitor rating (30 V)

Vers. A



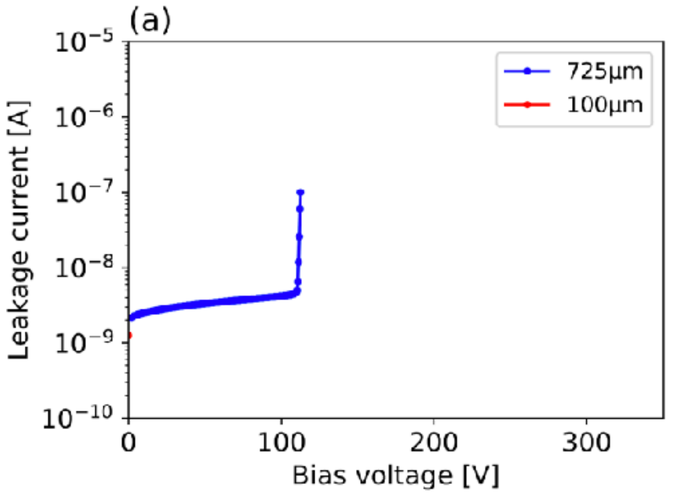
Vers. B

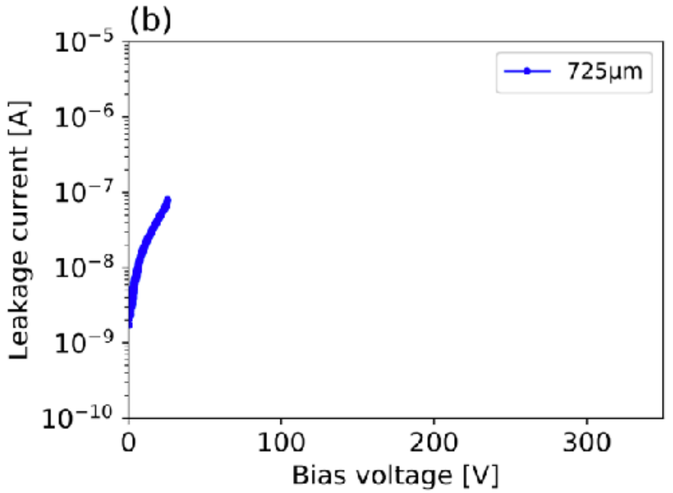


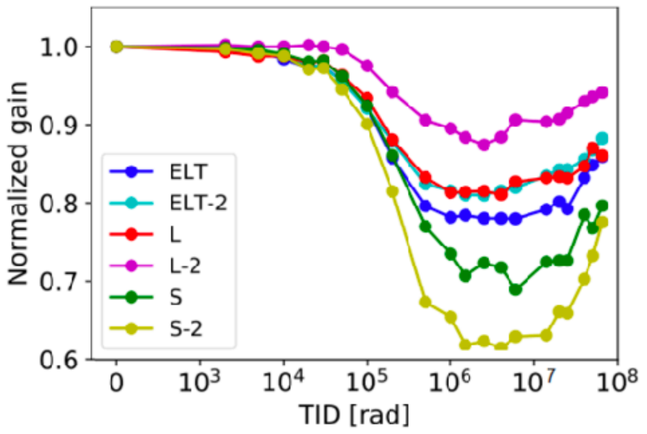
CCPD-LF (2014)

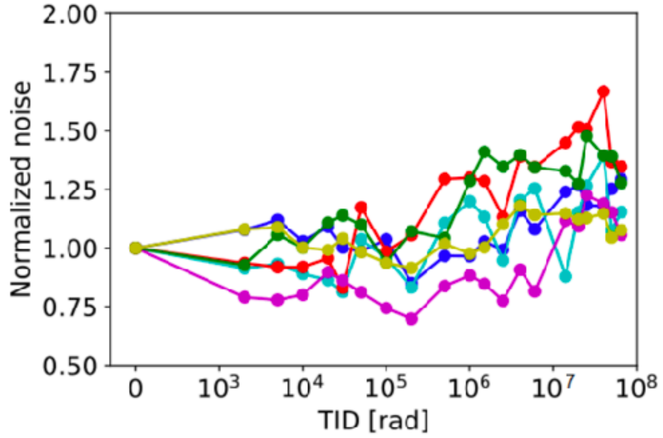
- Leakage current much higher in version B (small electrode), no breakdown visible
- Version A breakdown > 100 V
- Increase in noise after TID irradiation, drop in gain around 10 Mrad
- Size of transistor in feedback loop of CSA crucial for TID hardness

—> Decided for large transistor size and large collection electrode for demonstrator





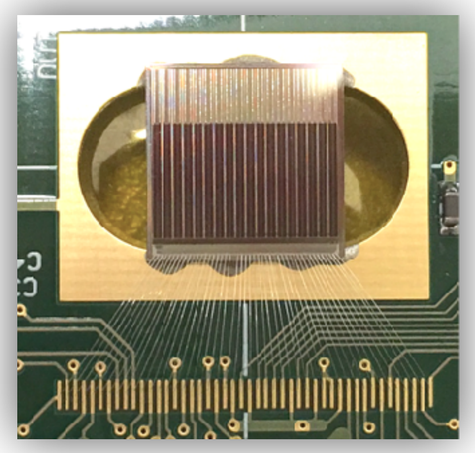




doi.org/10.1088/1748-0221/11/02/C02045
doi.org/10.1109/NSSMIC.2016.8069902

LF-CPIX (2016)

- Larger demonstrator based on CCPD-LF (150 nm LFoundry technology)
- Main purpose: evaluate and optimize performance of larger scale chips
- Hard facts:
  - Ca. 10 mm x 10 mm matrix size with 50 µm x 250 µm pixels
  - Different CSA implementations (NMOS, PMOS, CMOS)
  - Different spacing of innermost guard ring for improved breakdown

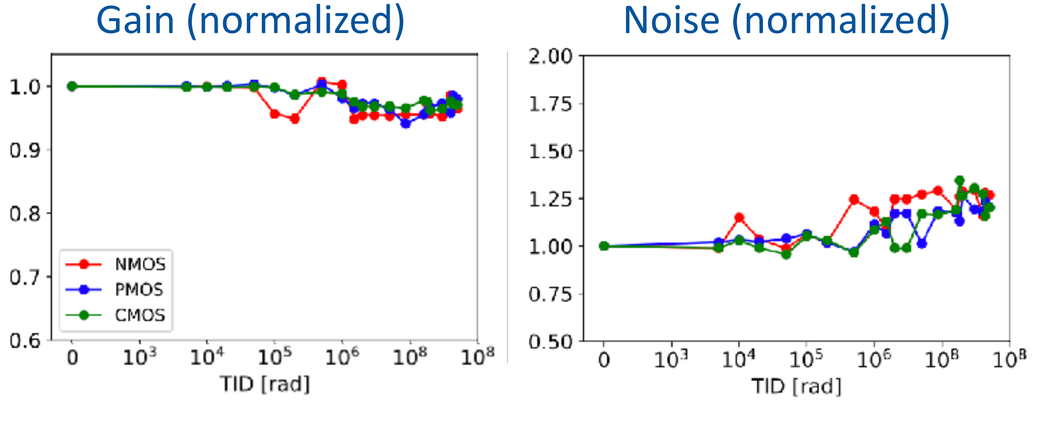


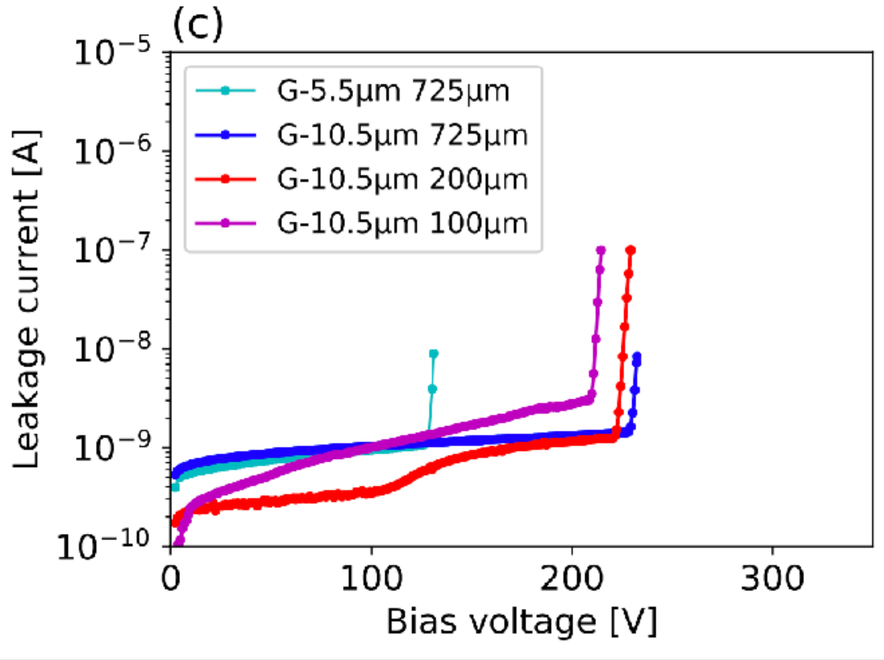
- Can be bump-bonded to FE-I4 due to matching pitch
- Charge measurement with FE-I4 or integrated comparator

doi.org/10.1088/1748-0221/11/12/C12064

LF-CPIX (2016)

- Increased spacing of innermost guard ring to n-ring almost doubles breakdown voltage to > 200 V
- Improvement of front-end significantly increases TID hardness



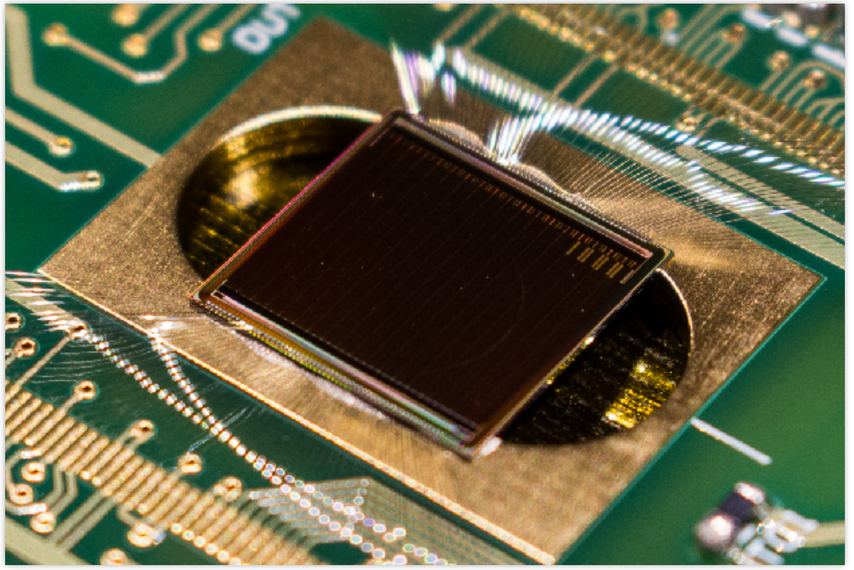


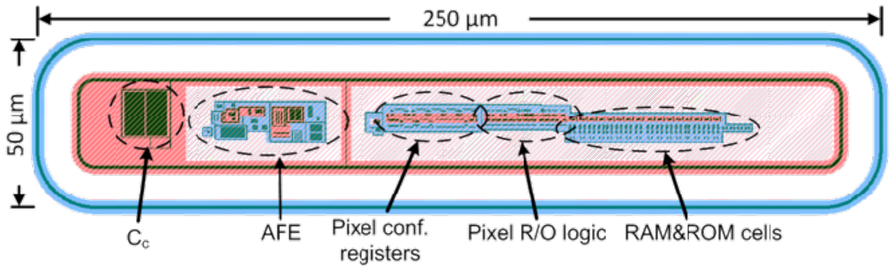
- CMOS CSA input shows good performance with low power consumption
- Implemented in most of the flavours in LF-Monopix1

doi.org/10.1016/j.nima.2018.10.059
T. Hirono, 2019

LF-MONOPIX1 (2017)

- First fully monolithic large scale prototype with integrated fast digital readout circuitry
- 10 mm x 10 mm matrix size with 50 µm x 250 µm pixels
- Nine pixel flavours of four columns each
- 4-bit in-pixel threshold adjustment
- Column-drain readout logic (FE-I3 like, used in ATLAS Inner Detector)
- 40 MHz BX clock with 7-bit TOT charge measurement
- Different CSA and discriminator implementations

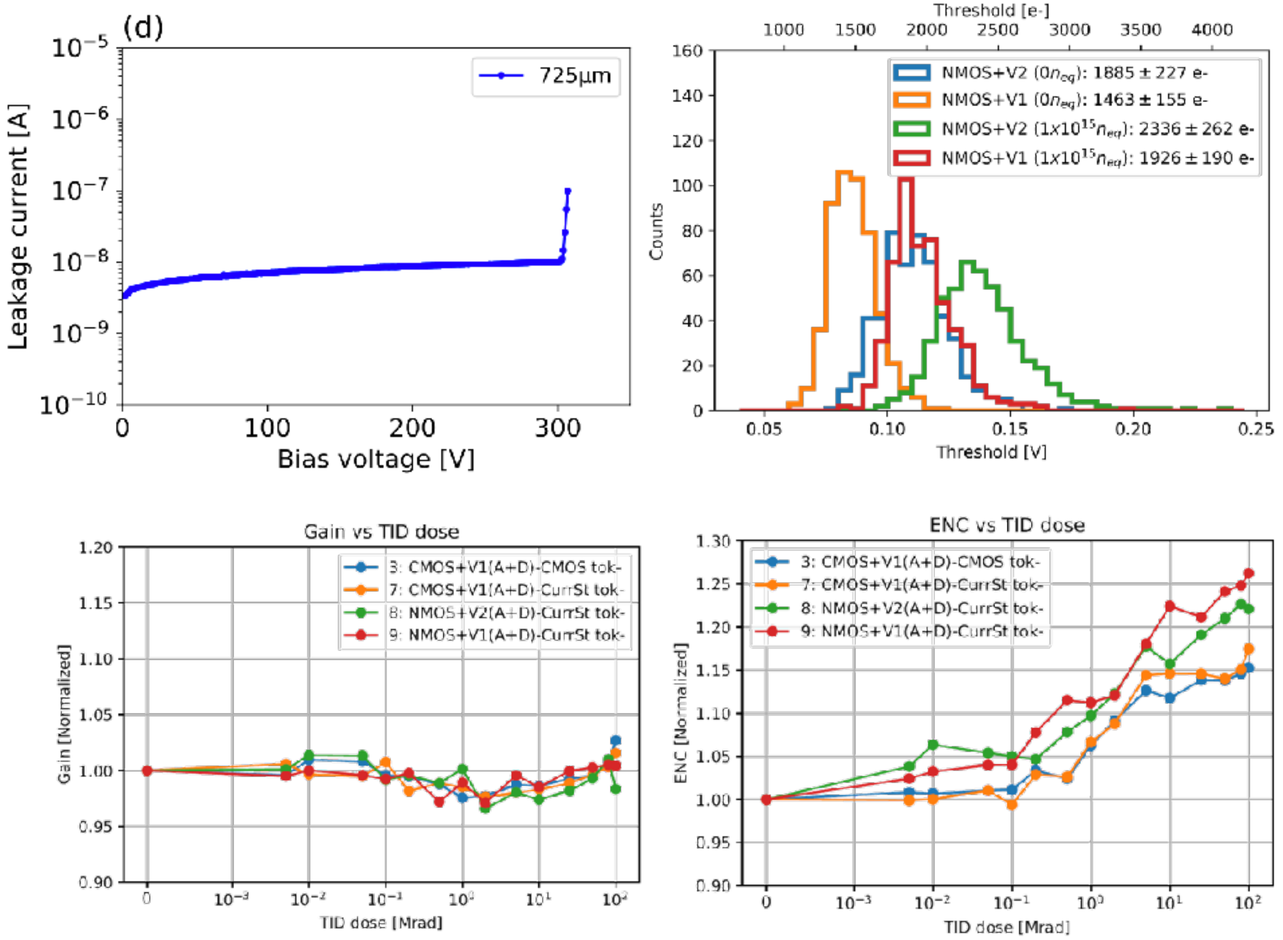




doi.org/10.1088/1748-0221/12/01/C01039

LF-MONOPIX1 (2017)

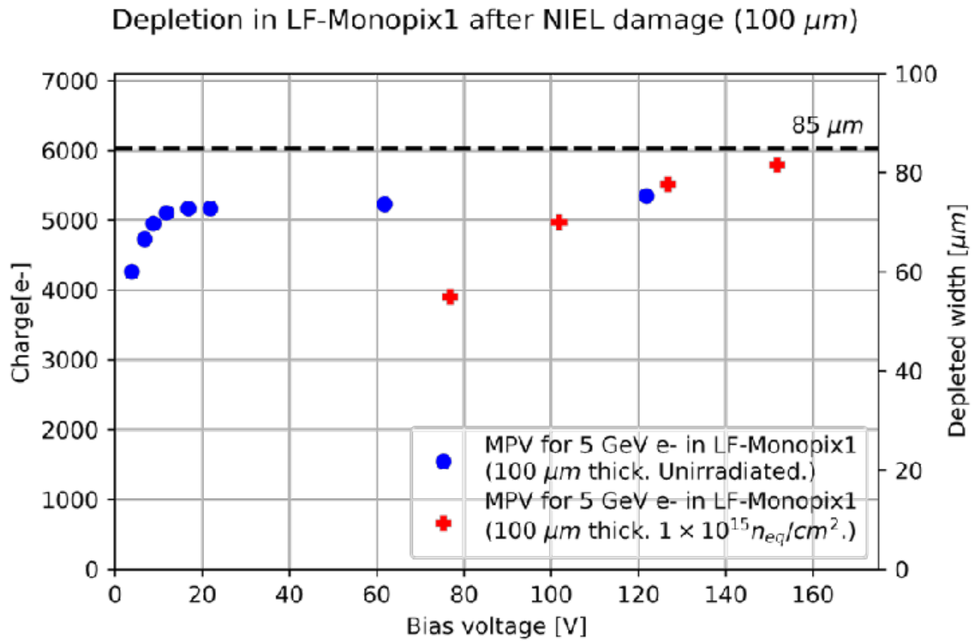
- Further increase of p-ring to n-ring distance for higher breakdown voltage (top left)
- Threshold before irradiation (10^{15} n_{eq}) < 2k e^-, after irradiation < 2.5k e^- (depends on flavour) top right: blue & green, orange & red
- New discriminator with good TID hardness (gain in bottom left, ENC in bottom right)
- Power consumption 55 µW / px | 1.7 µW / cm^2

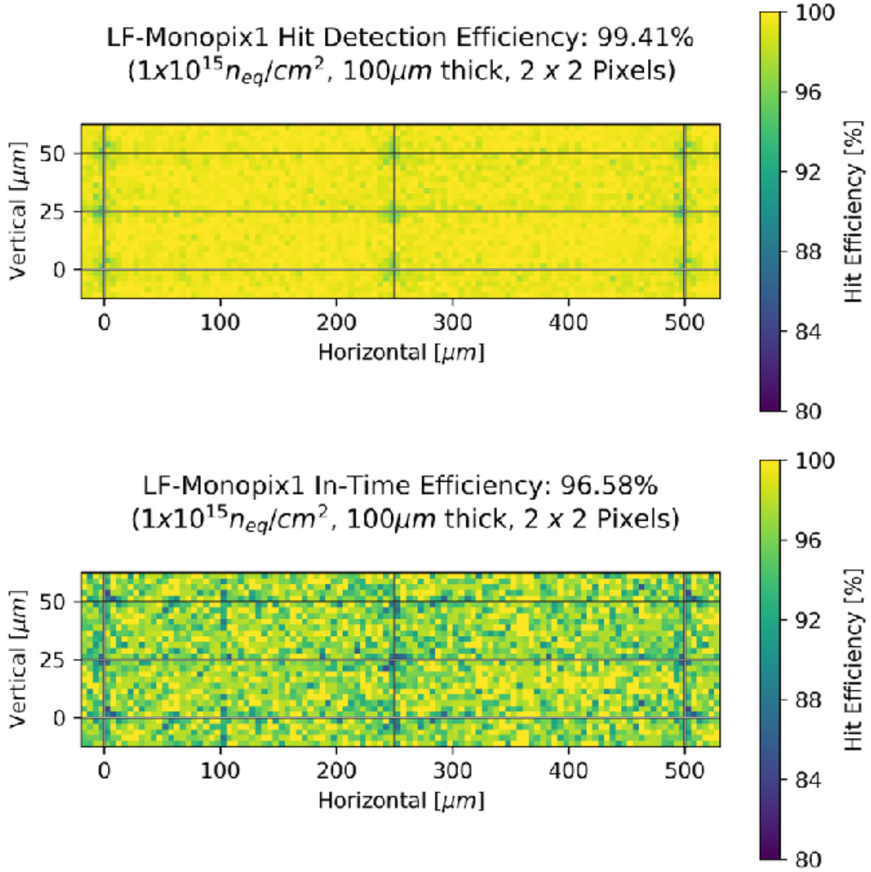


doi.org/10.1016/j.nima.2018.10.059

LF-MONOPIX1 (2017)

- Sensor tested after irradiation to 10^{15} n_{eq} in test beam at DESY
- 99.41 % hit detection efficiency & 96.58 % in-time efficiency
- 100 µm sample fully depleted after irradiation at 150 V

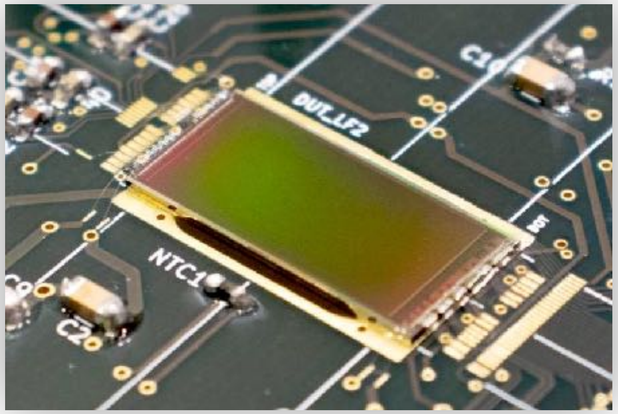


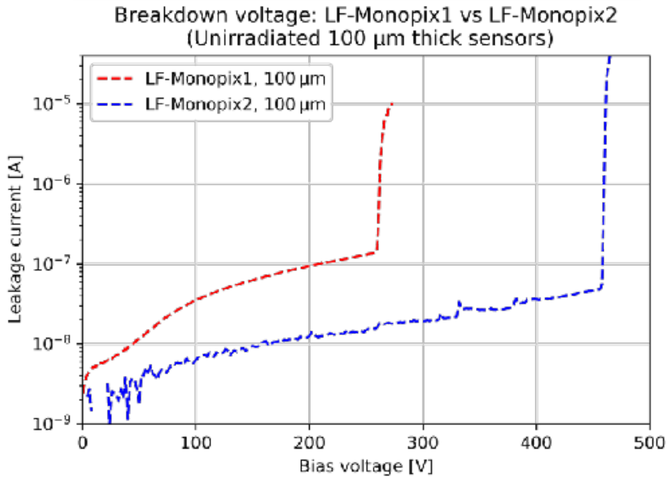


doi.org/10.1016/j.nima.2022.167224

LF-MONOPIX2 (2021)

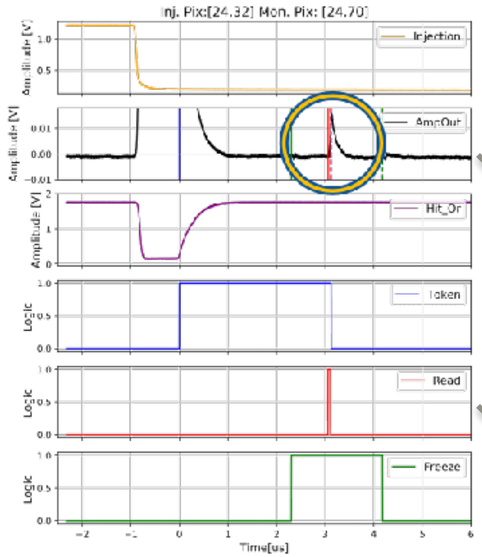
- Increased column length to 2 cm (i.e. „full-size“) at smaller pixel size
  - 50 x 150 µm pitch (minimum size in this design)
  - Further increase in breakdown voltage up to > 450 V
  - Power consumption of 28 µW per pixel
  - NMOS CSA and discriminator from LF-Monopix1 (best TID radiation hardness and speed)

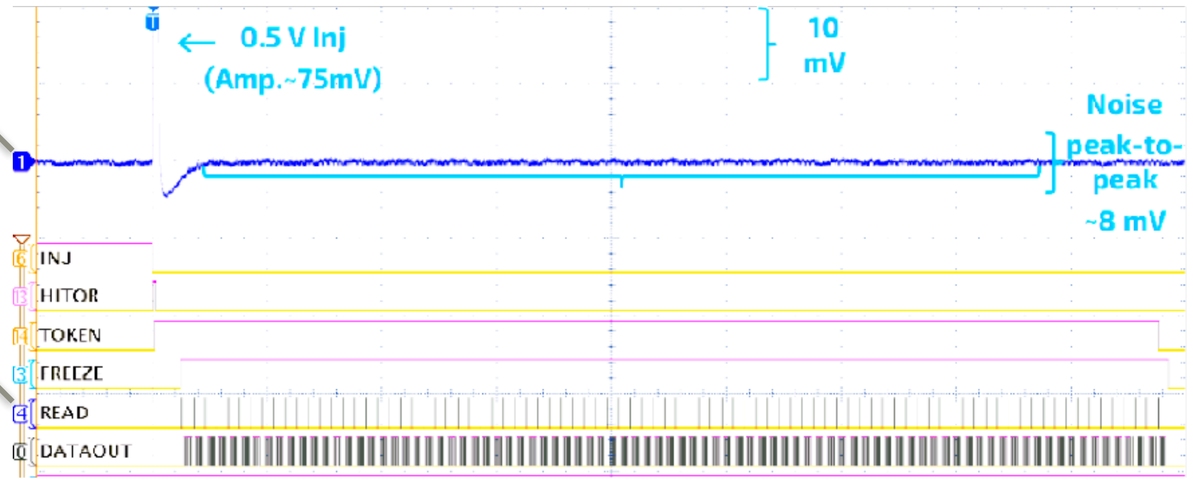


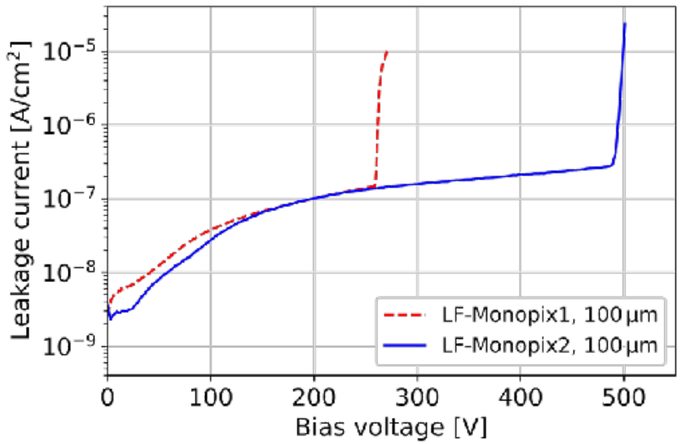


LF-MONOPIX2 (2021)

- Observed coupling from digital signal (READ of column drain logic) to front-end input
- Similar behaviour already present in LF-CPIX with shift register toggling
- Mitigated with new layout, restricts pixel size

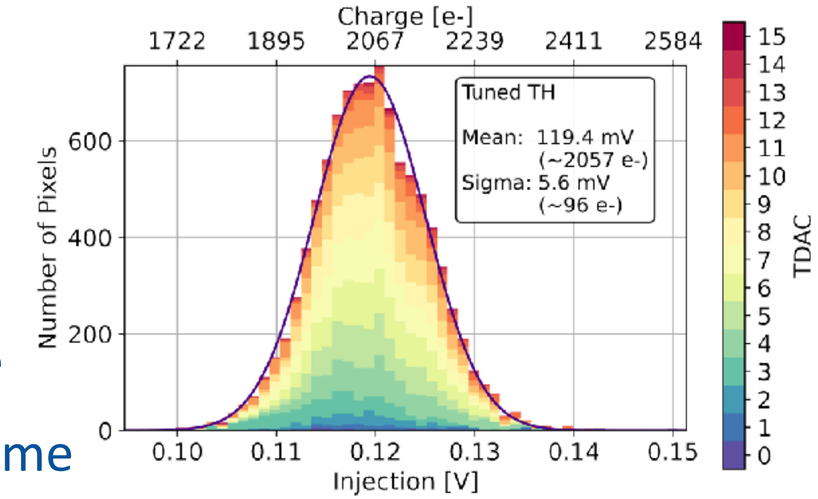


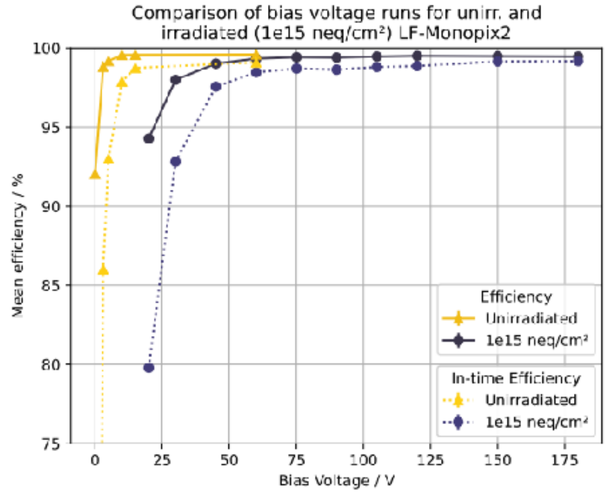




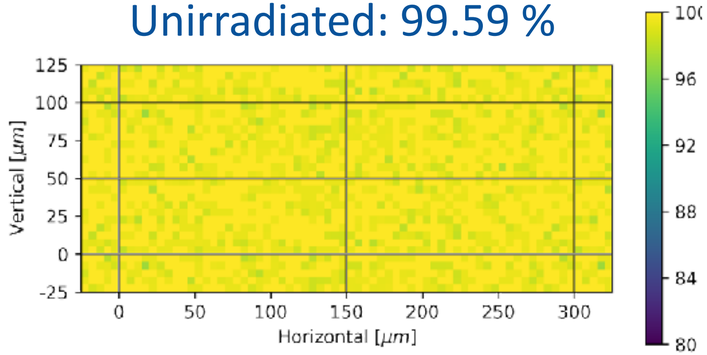
LF-MONOPIX2 (2021)

- Smaller pixel pitch results in lower ENC —> low threshold (top left)
- Very high and homogeneous efficiency, also after fluence of 10^{15} n_{eq}
  - before irradiation: 99.43 % hits in-time
  - After irradiation: up to 99.8 % hits in-time (depending on matrix flavour, > 99 %)
  - Significant improve from LF-Monopix1, due to lower capacitance and ENC
- Characterisation ongoing, samples with 2 x 10^{15} n_{eq} available

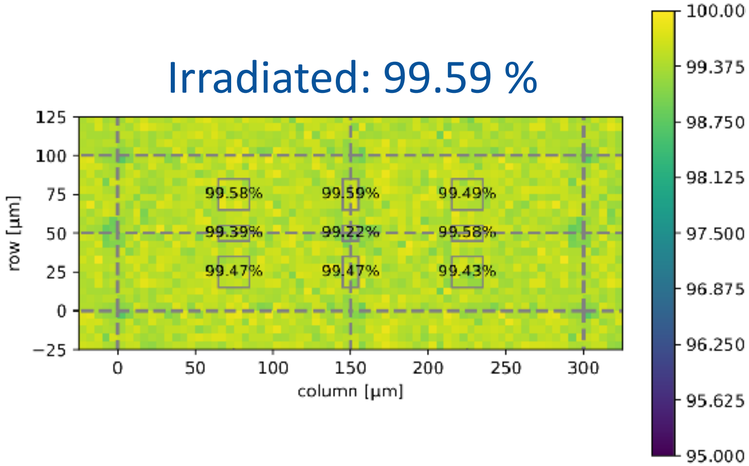




Unirradiated: 99.59 %



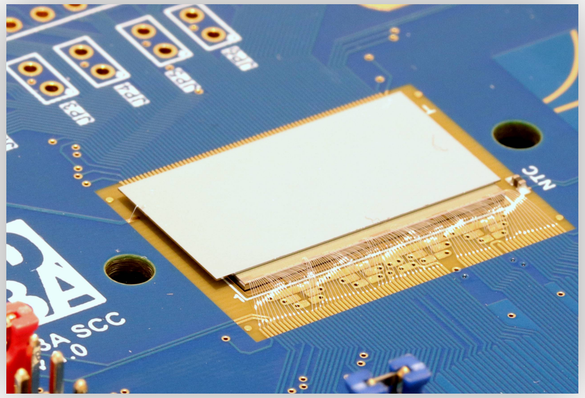
Irradiated: 99.59 %

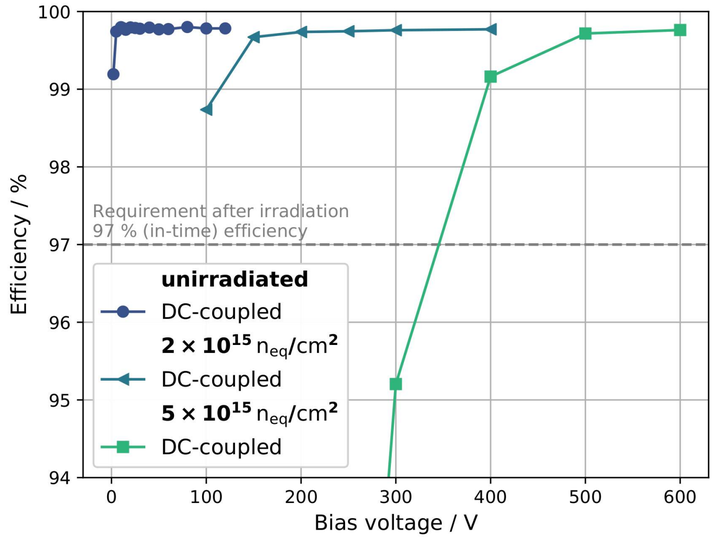


doi.org/10.1016/j.nima.2022.167224
VERTEX 2022 proceedings accepted

LFOUNDRY PASSIVE CMOS SENSORS

- Commercial CMOS processes offer features useful for pixel sensors:
  - Multiple metal layers (AC coupling)
  - Large wafers, high production through-put at low cost
  - And more…
- Bonded to ATLAS ITk pixel readout chip for testing
- Breakdown voltage > 600 V after irradiation
- At 5 x 10^{15} n_{eq} fluence: > 99 % in-time efficiency





—> Suitable for large area detectors In very harsh radiation environments

doi.org/10.1016/j.nima.2021.165771

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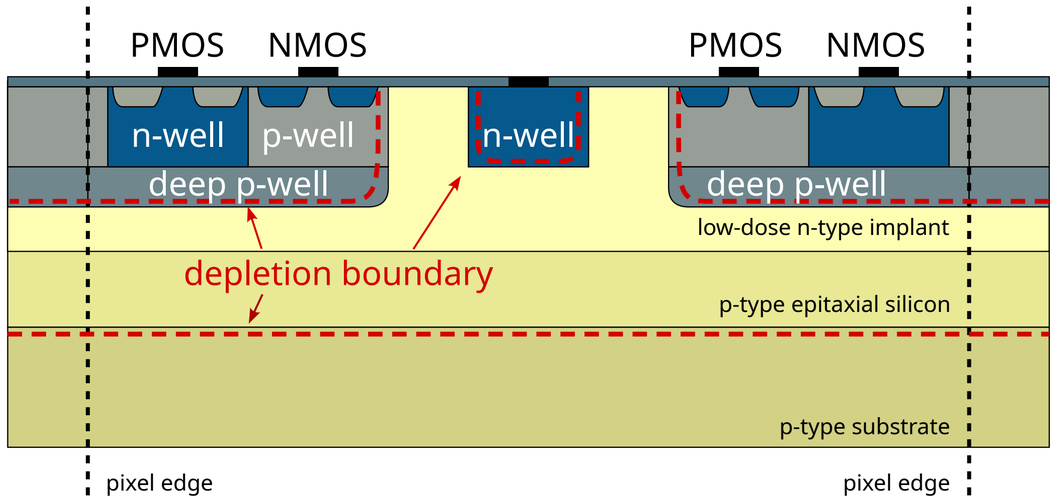
TJ-MONOPIX

A NEW DEVELOPMENT IN A TOWERSEMI 180 NM CMOS PROCESS

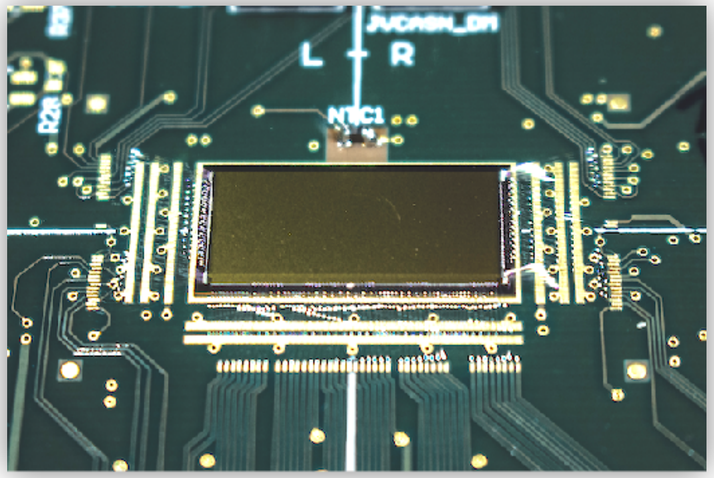
- Originally designed for ALPIDE chip for ALICE upgrade, adapt for DMAPS with ATLAS pixel requirements
- 180 nm process with modifications to fully deplete the sensor material for fast charge collection by drift and increased radiation hardness
- Low-dose n-type implant developed together with foundry creates horizontal depletion boundary for homogeneous depletion
- Parallel development from Bonn & CERN (MALTA chip) after initial prototypes and demonstrator



doi.org/10.1016/j.nima.2017.07.046

TJ-MONOPIX1 (2018)

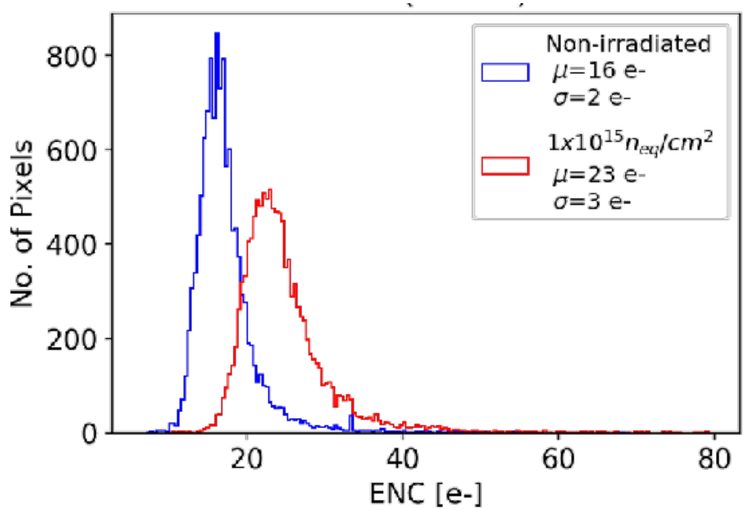
- Small collection electrode design (4 fF capacitance)
- Same column-drain readout as LF-Monopix (as opposed to TJ-MALTA from CERN group)
- 36 x 40 µm pixel pitch in a 1 x 2 cm matrix (four flavour variations)
- Built on 25 or 30 µm epitaxial silicon layer, substrate thinned to 100 µm
- Because of design limitations, maximum voltage of 6 V
- No in-pixel threshold adjustment, readout circuitry based on ALPIDE as well



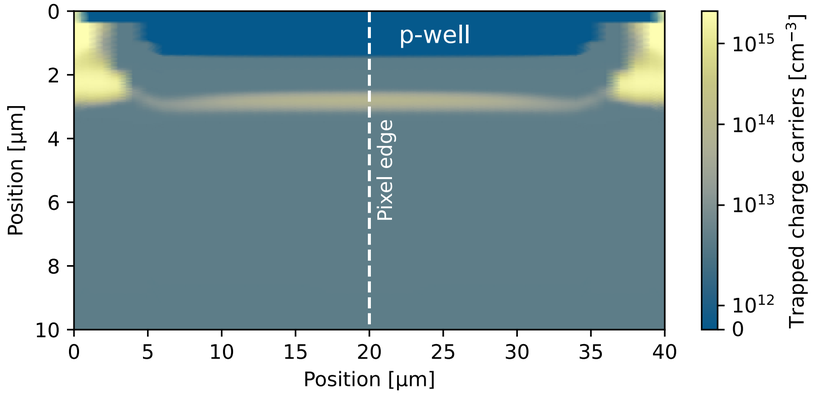
K. Moustakas, 2021

TJ-MONOPIX1 (2018)

- Observed tail (later attributed to RTS) in noise distribution
  - Limited minimum threshold to > 350 e, larger than design
  - Signal (especially after irradiation too small)
  - Original design 70 % efficiency at 10^{15} n_{eq} -> redesign of sensor for better field shape and samples with 100 µm Cz silicon
  - Still, need more charge (Cz) or lower threshold for > 99 %



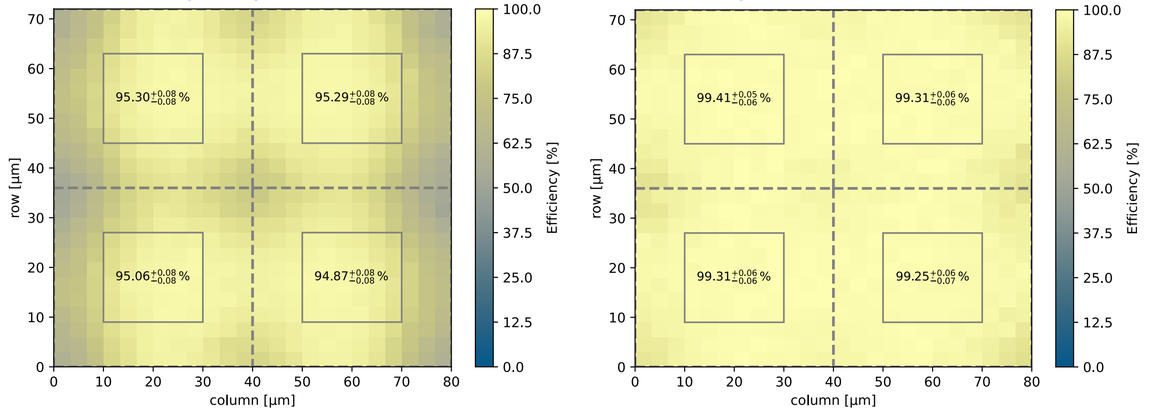
qualitative TCAD simulation



Improved sensor geometry

30 µm epitaxial

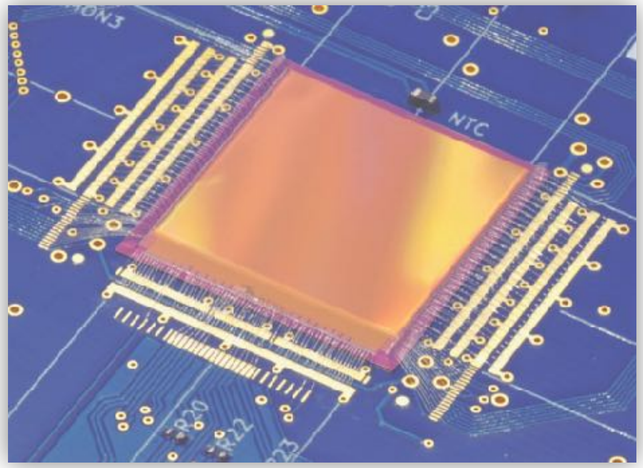
100 µm Czochralski

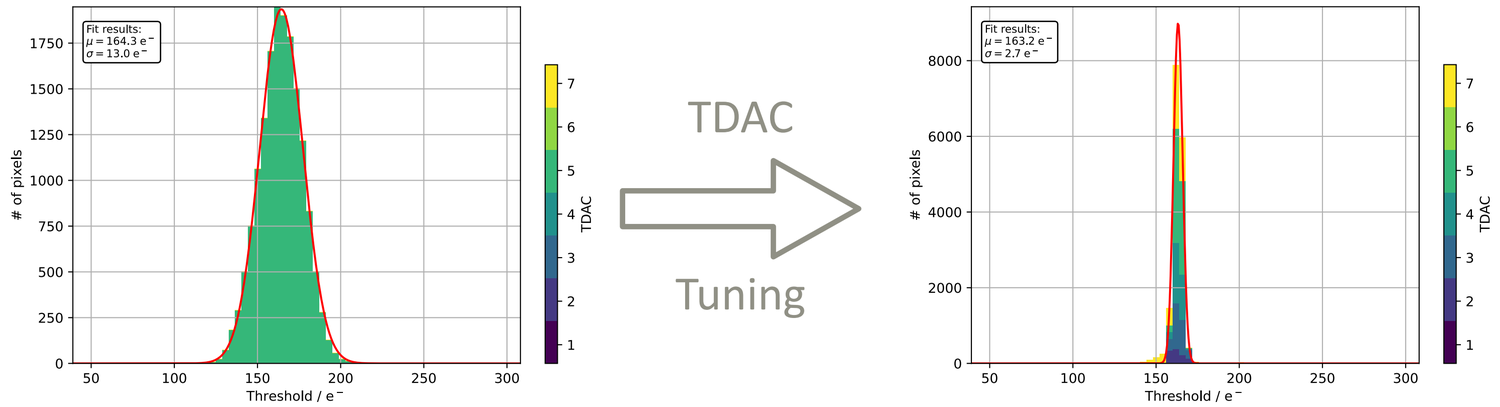


doi.org/10.1088/1748-0221/14/05/C05013

TJ-MONOPIX2 (2021)

- Improved in-pixel electronics for lower threshold and less noise
- Pixel size 33 x 33 µm, chip size 2 x 2 cm (512 x 512 pixels)
- Mature periphery with configuration registers, readout, LVDS RX/TX
- Command protocol from RD53, 8b10b encoded data (triggerless)
- Added 3-bit threshold tuning on pixel level
  - Threshold dispersion < 3 e
  - Threshold O(200 e)
  - Noise ≈ 5 e

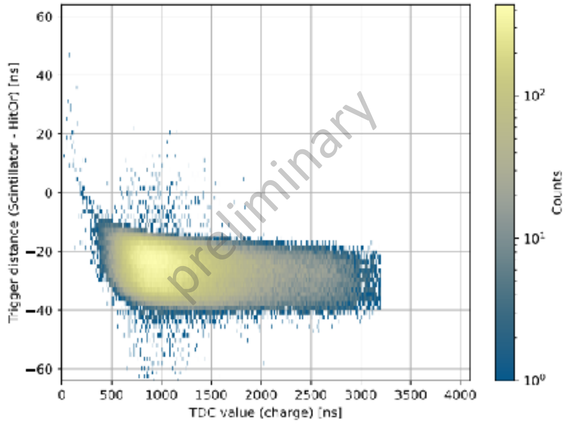


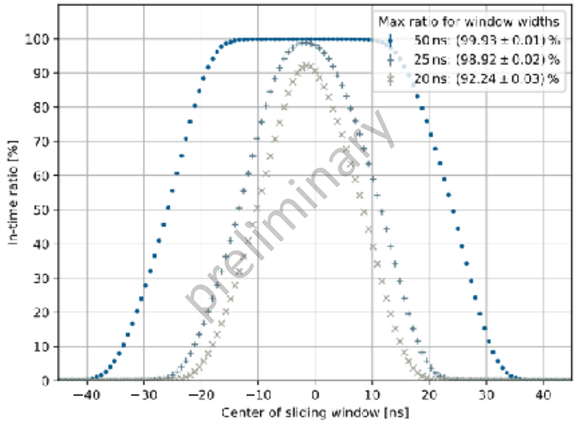


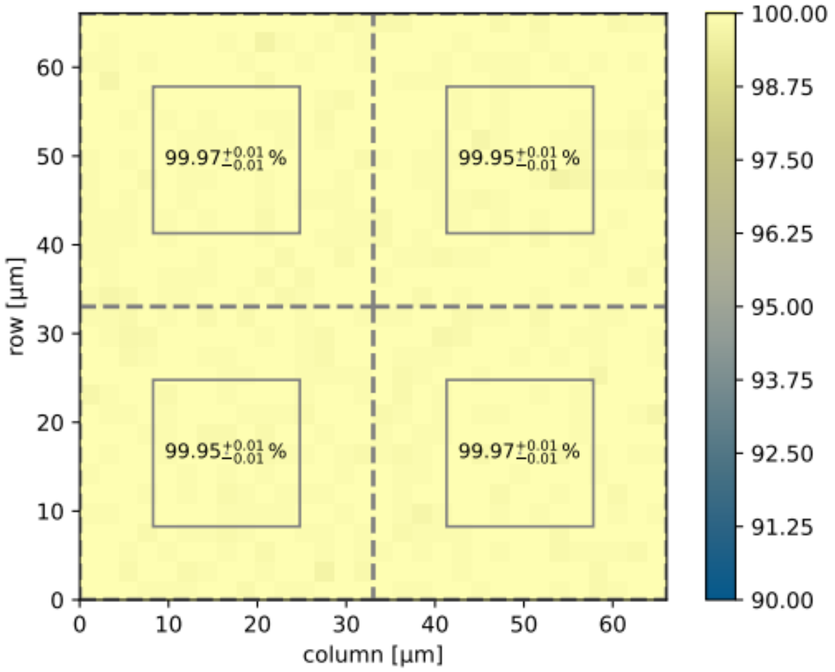
doi.org/10.1016/j.nima.2022.167189

TJ-MONOPIX2 (2021)

- Efficiency before irradiation > 99.9 % on 30 µm epi silicon
- Average cluster size > 1.5, for 100 µm Cz > 2
  - Spatial resolution better than p / sqrt(12): < 10 µm
- 98.92 % of hits within 25 ns (analysis ongoing)





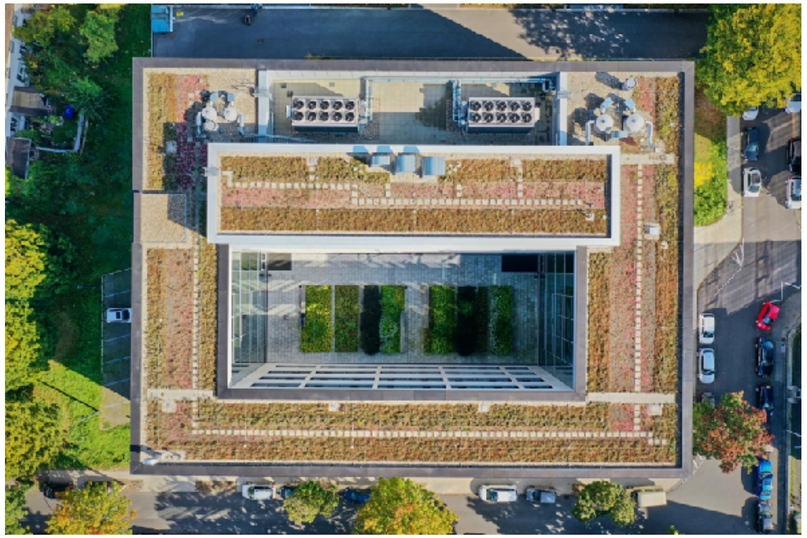


- Characterisation ongoing, irradiated samples recently available

doi.org/10.22323/1.420.0080

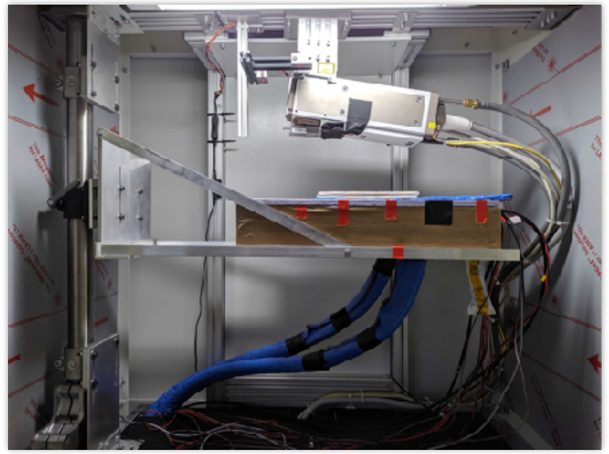
BONN AS TESTING SITE

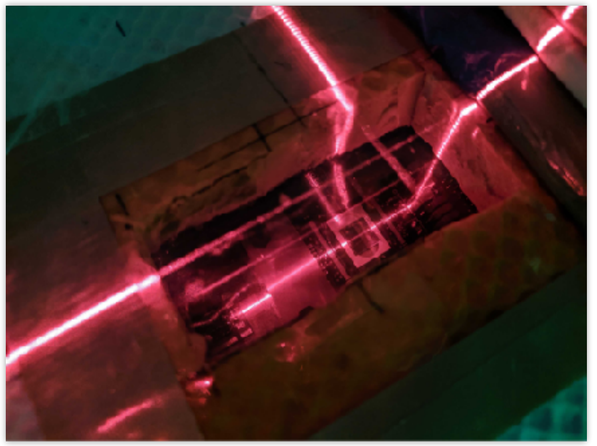
- New research facility since 2021: synergy of different detector groups
  - silicon, TPC, MPGD, nanophotonics, ASIC design
- Deep underground laboratory, electronics and mechanical workshop, 360 m^2 clean room area (ISO5 - 7)
- Multiple wirebonding machines, wafer probing stations, MPGD production

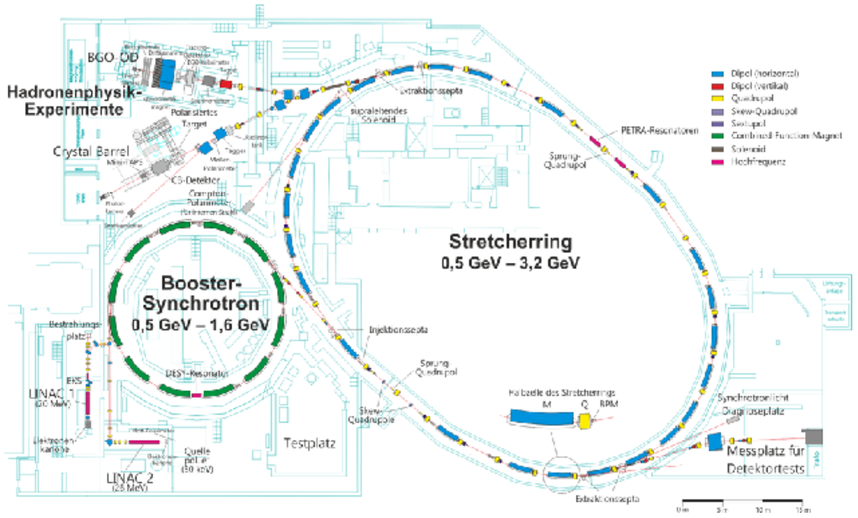


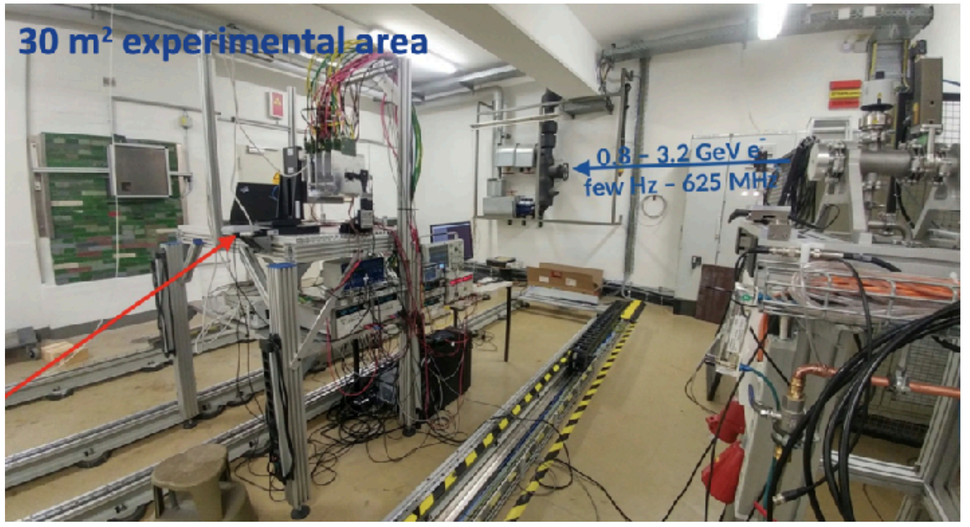
BONN AS TESTING SITE

- X-ray irradiation machine (TID testing)
- Electron accelerator ELSA in neighbouring building
  - 3.2 GeV polarised electrons
  - External beamline for detector tests with primary electrons (up to 625 MHz rate)



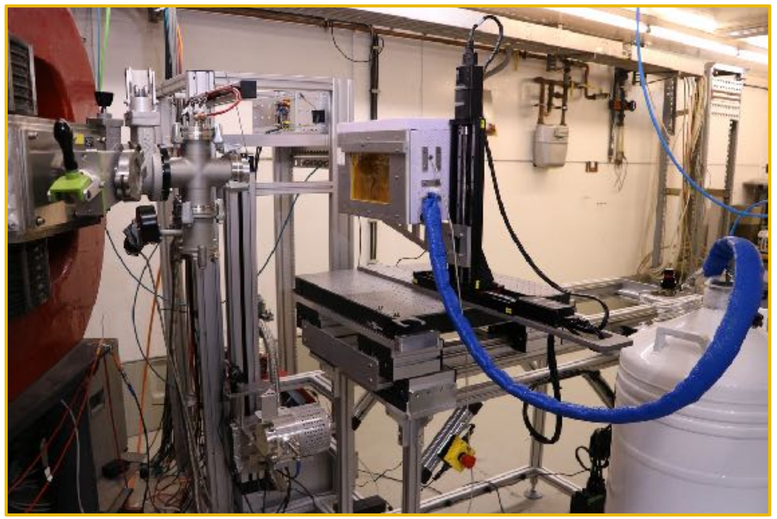


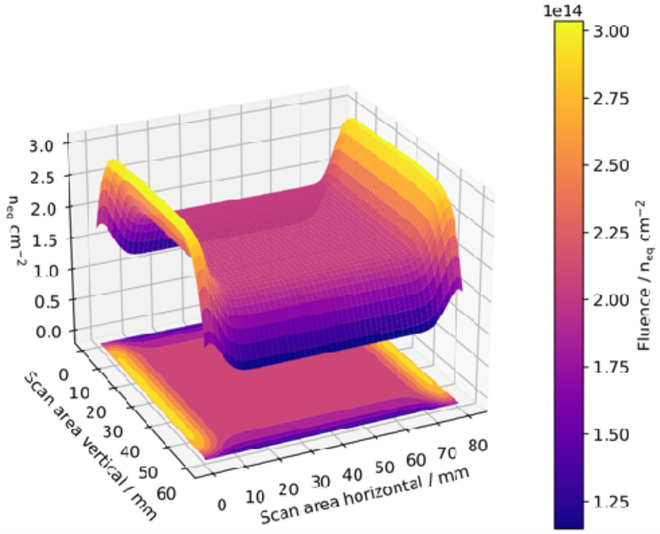




BONN AS TESTING SITE

- Irradiation site for Si-detectors at Bonn Isochronous Cyclotron
- 14 MeV protons with hardness factor of $\kappa_p = 3.7$
- Between 1e12 and 5e13 neq/cm² per application
- Irradiation in cold (< -20°C) box, powering/readout possible
- Beam-based dosimetry and scan routine yields highly-uniform fluence distribution with low uncertainty
- Low energy limits DUT thickness:
  - Up to 300 µm Si best to ensure constant damage over depth





doi.org/10.18429/JACoW-IPAC2022-MOPOST030

CONCLUSION

- Long development of depleted monolithic active pixel sensors in commercial CMOS processes
- Common design goal: ATLAS ITk outer pixel layer (but no DMAPS made the cut in 2018)
- Two large-scale chips currently under investigation with promising results
  - High hit detection and timing efficiencies
  - Mature digital readout in matrix and advanced functionality in periphery
  - Characterisation ongoing, irradiated samples (NIEL) to different fluences available, TID irradiations planned for Q1 2024

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

This project has received funding from the Deutsche Forschungsgemeinschaft DFG (grant WE 976/4-1), the German Federal Ministry of Education and Research BMBF (grant 05H15PDCA9), and the European Union's Horizon 2020 research and innovation program under grant agreements no. 675587 (Maria Sklodowska-Curie ITN STREAM), 654168 (AIDA-2020), and 101004761 (AIDAinnova).

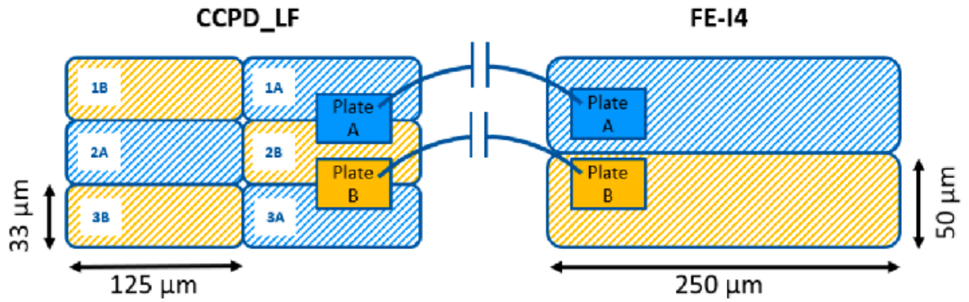
UNIVERSITÄT BONN

SI LAB
Silizium Labor Bonn

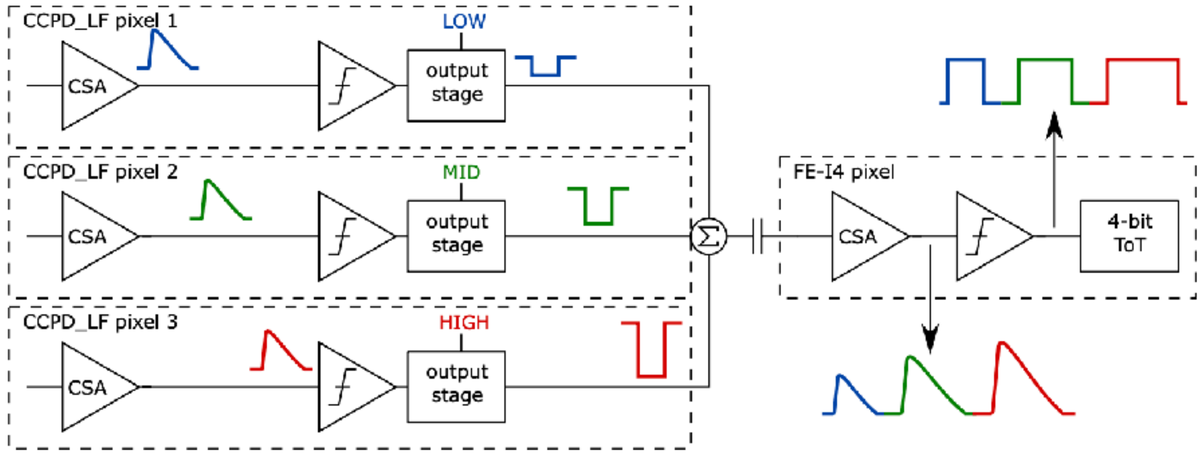
BACKUP

CCPD-LF COUPLING

- Output stage modulates pulse height
- Differentiate pixel by measured „charge“ in FE-I4
- Glue bonding (AC coupling)



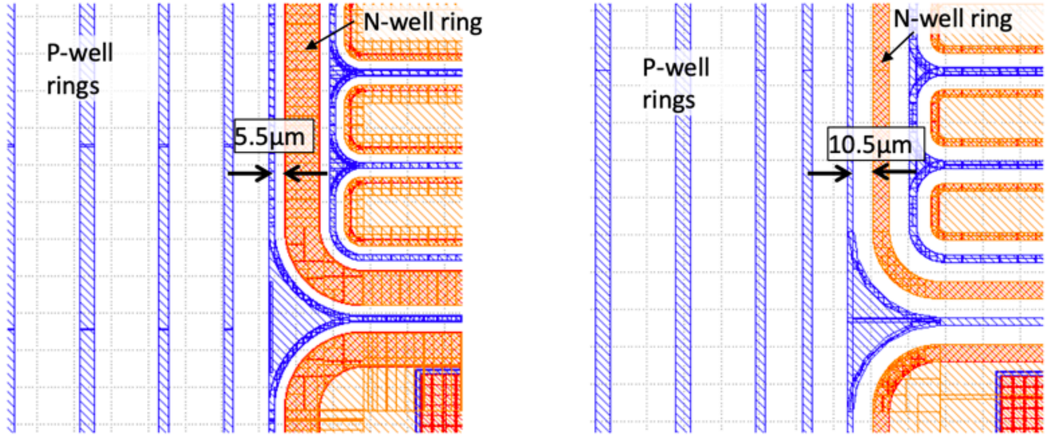
(a) Arrangement of connections between a group of six pixels of CCPD_LF and two pixels of FE-I4.



(b) Illustration of the idea of sub-encoding CCPD_LF pixels using programmable pulse height. Based on [60]

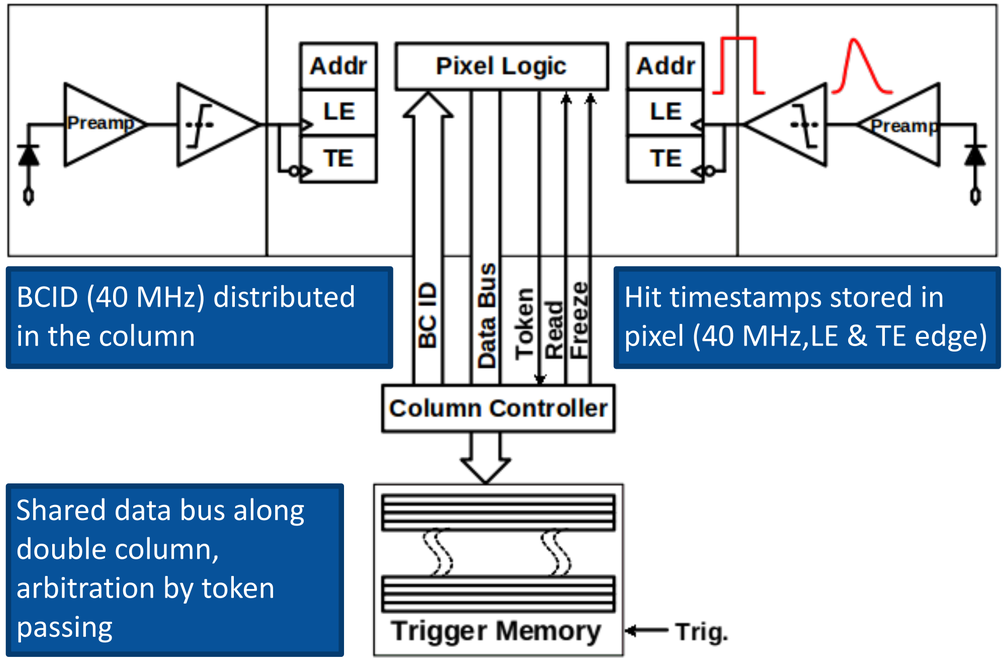
LF-CPIX

- Guard ring spacing 5.5 µm increased to 10.5 µm



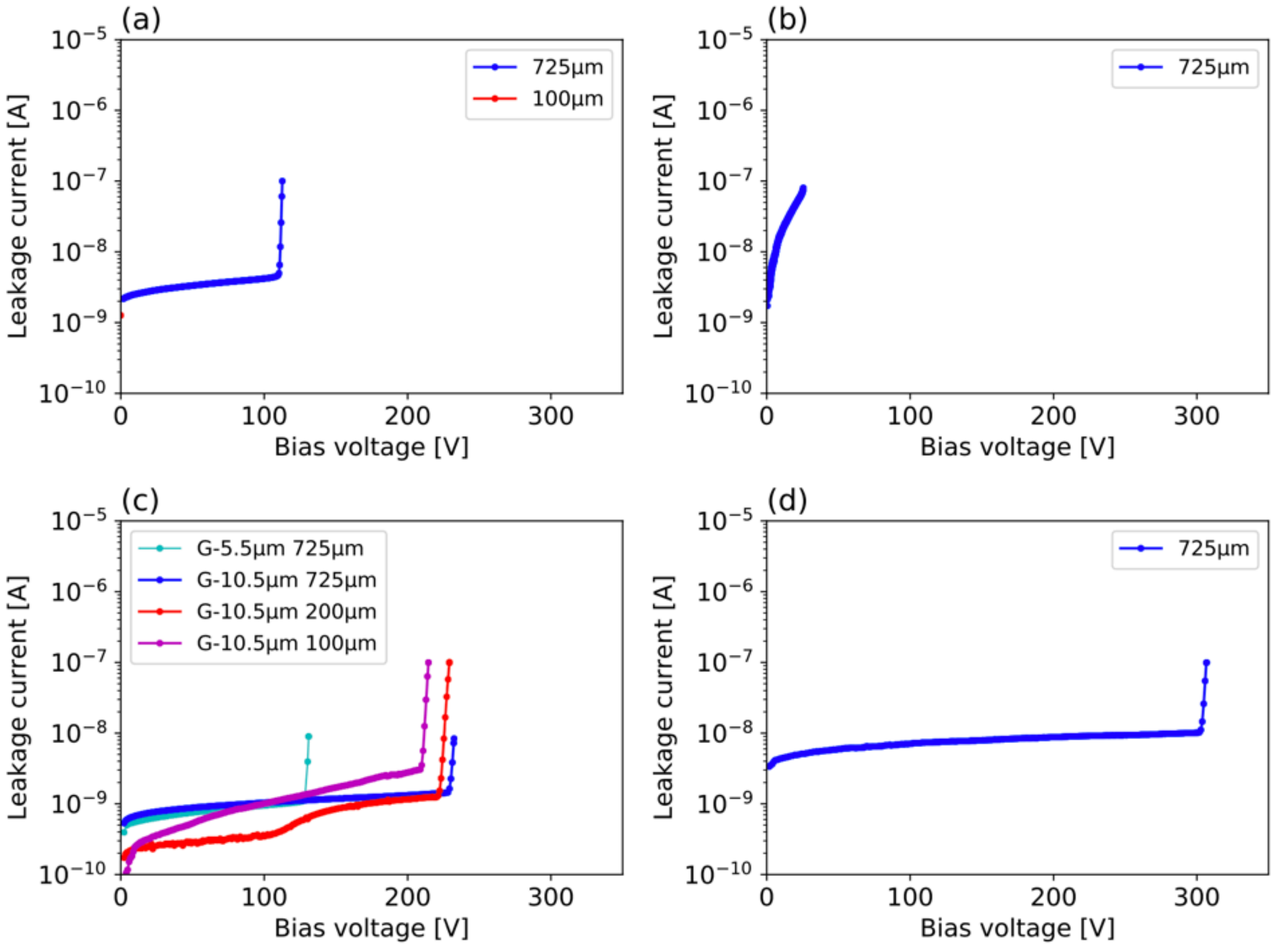
COLUMN DRAIN READOUT

- Used in FE-I3, proven to cope with ATLAS pixel detector hit rate
- Simulations show ATLAS ITk outer layer capabilities



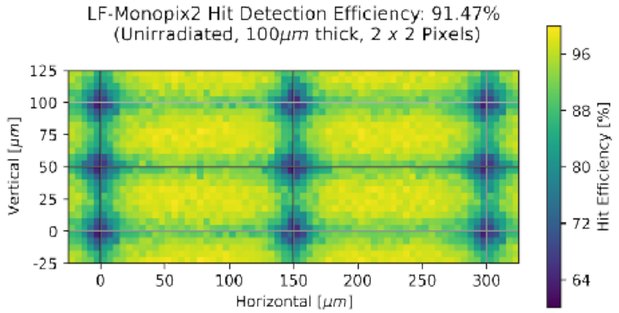
BREAKDOWN VOLTAGE LFOUNDRY

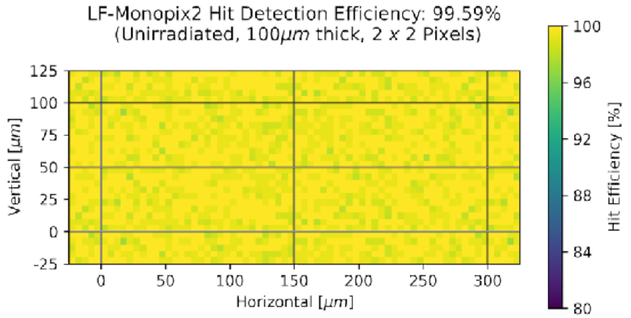
A. CCPD-LF (large collection electrode)
B. CCPD-LF (small collection electrode) limited by AC coupling capacitor
C. LF-CPIX (different p-ring to n-ring spacing)
D. LF-Monopix1

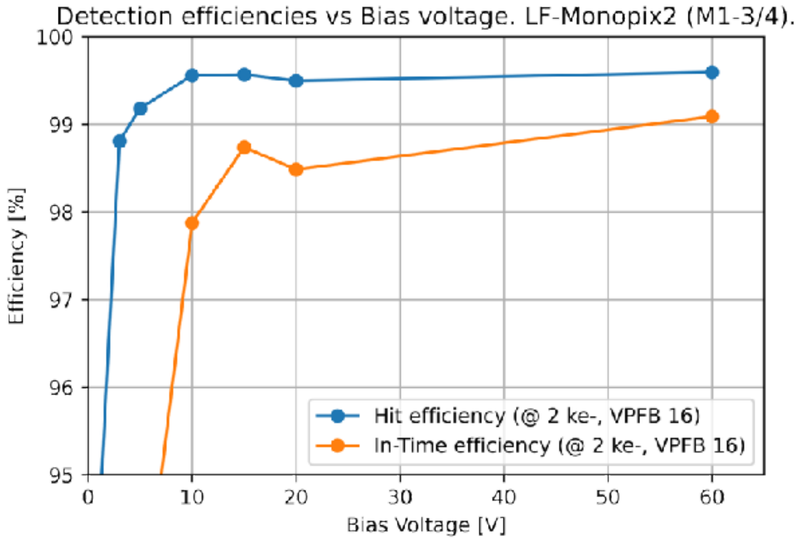


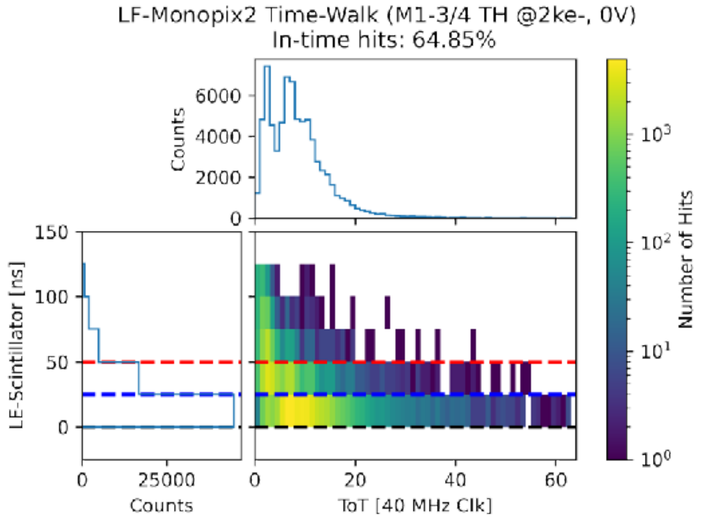
LF-MONOPIX2 EFFICIENCY

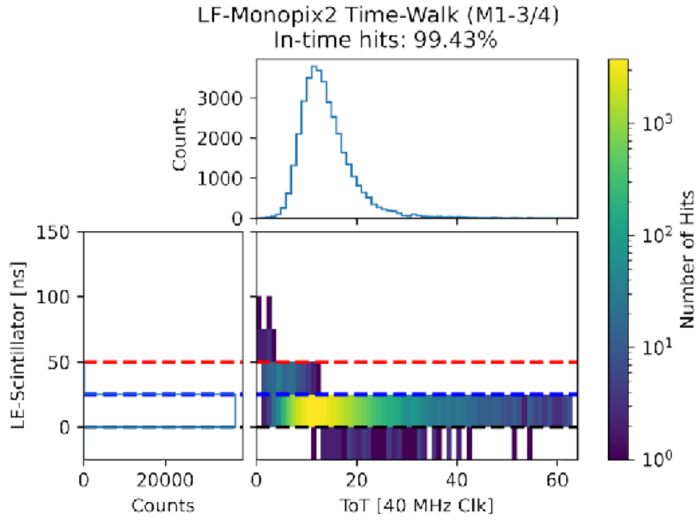
- 0 V bias (left) vs 60 V bias (right)
- Expected drop for small bias
- Losses in pixel corners and edges





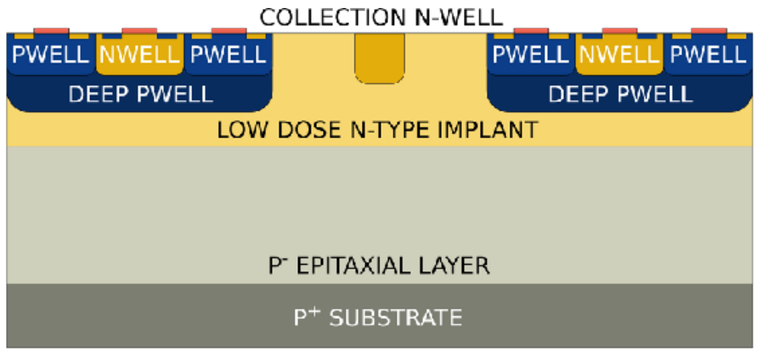


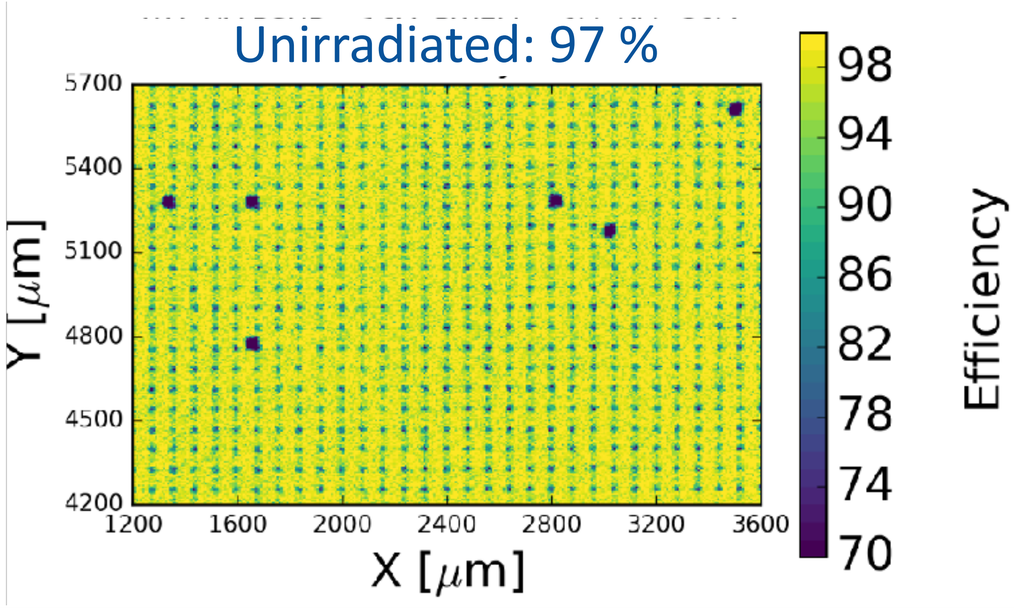


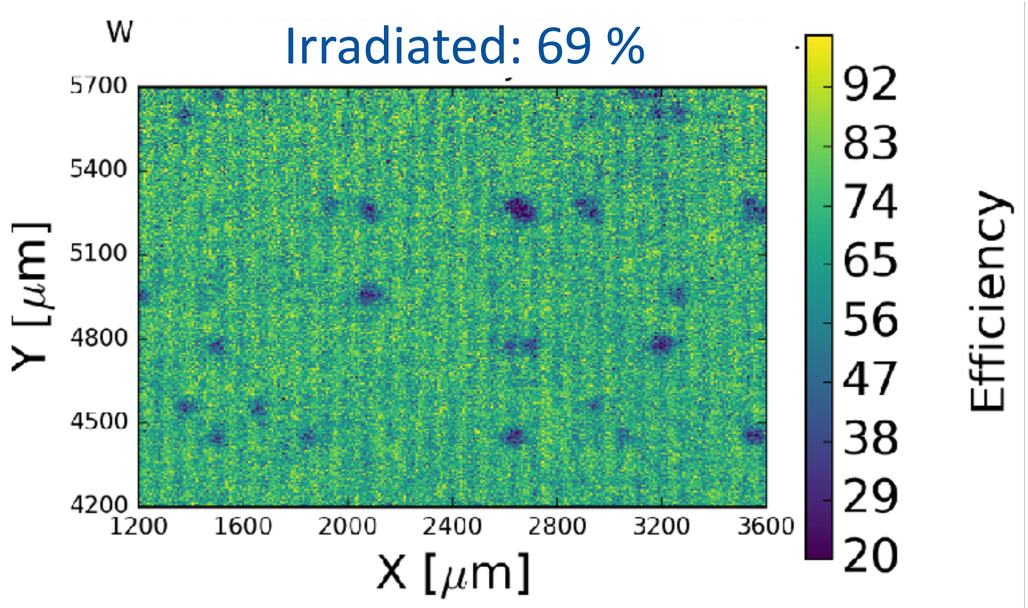


TJ-MONOPIX1 INEFFICIENCY

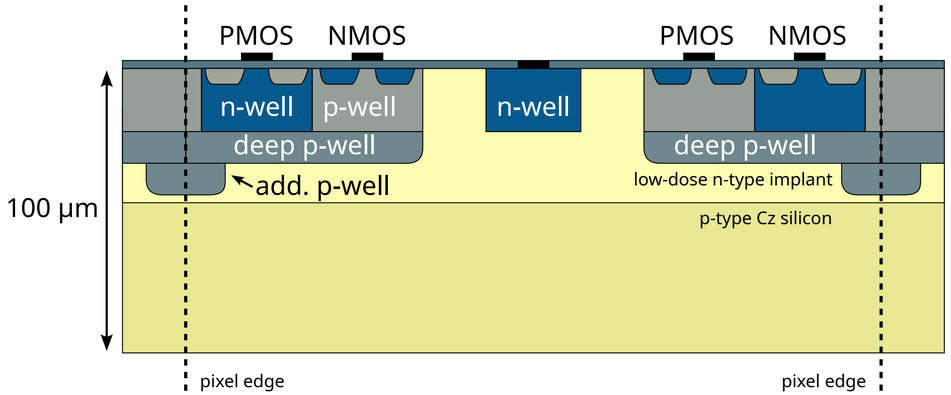
- Significant efficiency loss after irradiation
  to < 70 % (at $10^{15}\,\mathrm{neq\,cm^{-2}}$)
- Charge is lost due to E-field shaping under deep pwell
  -> need another modification besides low dose n-type

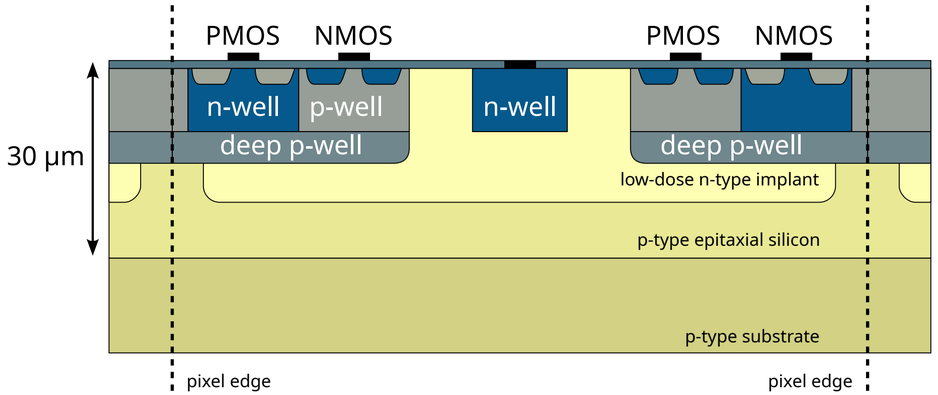


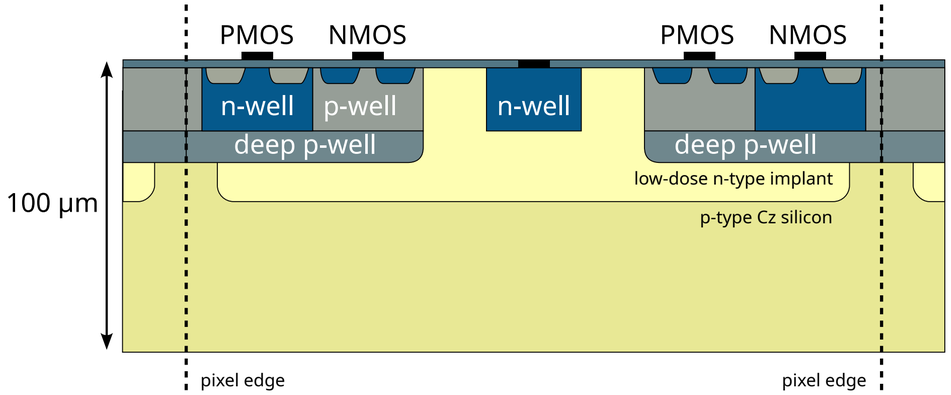


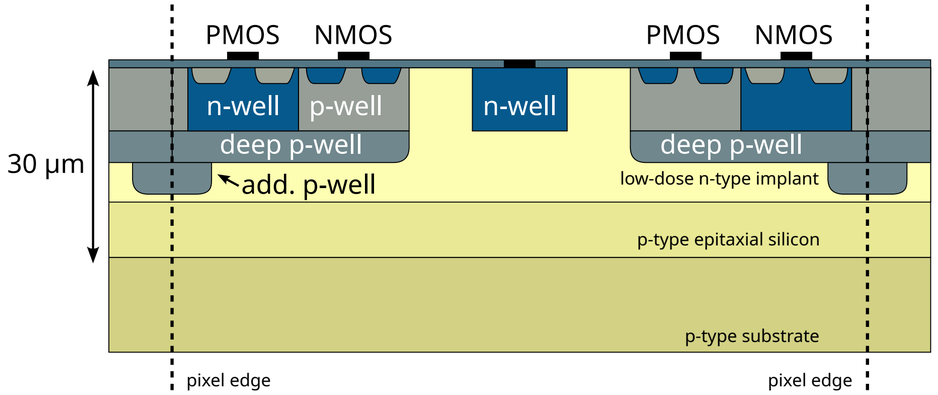


TJ-MONOPIX1 / TJ-MONOPIX2 GEO









DETECTOR REQUIREMENTS

	ALICE LHC	ATLAS HL-LHC		Belle II SuperKEKB
		Outer	Inner	
Time resolution [ns]	20 000	25	25	(100)
Particle rate [kHz / mm^2]	10	1000	10 000	1500
Fluence [neq cm^{-2}]	> 10^{13}	10^{15}	2 x 10^{16}	10^{14}
Ion. Dose [MRad]	0.7	50	> 1000	100

Design specification for rad-hard DMAPS

DMAPS potential candidate