

CMS silicon detector upgrade

Imperial College
London

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on behalf of the CMS Tracker group



Current and future tracking and vertexing detectors 2023 - QMUL London

8 November 23



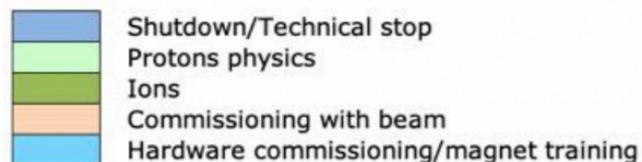
HL-LHC (Phase2) schedule

Specs

- **High Luminosity upgrade** after LS3
- Peak Luminosity $\sim 7.5 \times 10^{34} \text{ cm}^{-1}\text{s}^{-1}$
- **Expected Pile-up ~ 200** (current one designed for 20)
- Higher rates and radiation dose than Run3
- **Final integrated luminosity 3-4 ab^{-1}**
- 10x more radiation (up to 1.2 Grad, fluence of $2.3 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$)



Last updated: January 2022



Phase2 CMS detector overview

L1 Trigger HLT/DAQ

- Tracks in L1-Trigger at 40 MHz
- PFlow selection 750 kHz L1 output
- HLT output 7.5 kHz
- Latency within 12.5 μ s
- 40 MHz data scouting

Endcap Calorimeter (HGCAL)

- 3D showers and precise timing
- Si, Scint+SiPM in Pb/W-SS

Barrel Calorimeter

- ECAL crystal granularity readout at 40 MHz
- with precise timing for e/ γ at 30 GeV
- ECAL and HCAL new Back-End boards

MIP Timing Detector

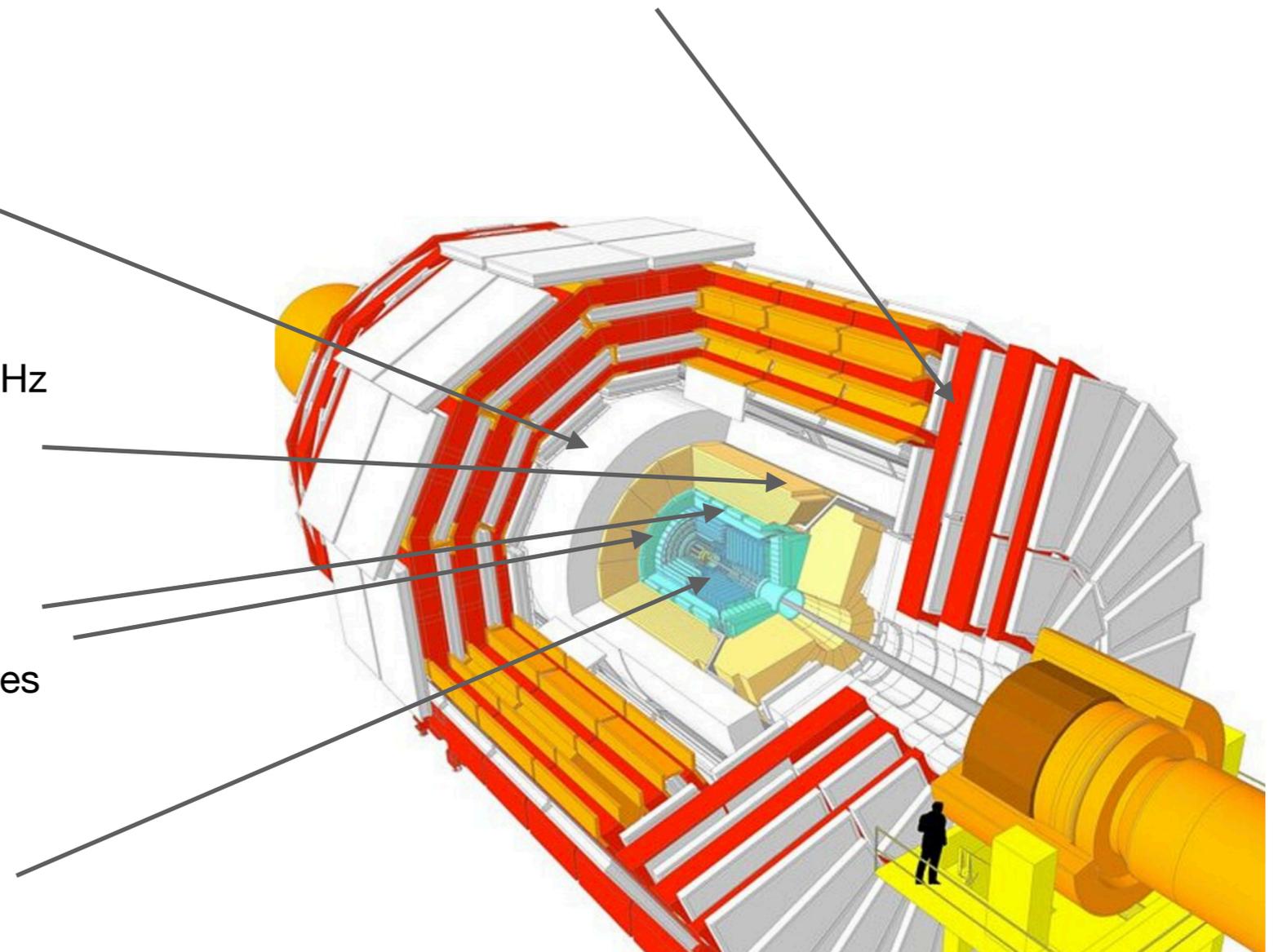
- Barrel layer: Crystals + SiPMs
- Endcap layer: Low Gain Avalanche Diodes

Tracker

- Increased granularity
- Design for tracking in L1-Trigger
- Extended coverage to $\eta \approx 4$

Muon Systems

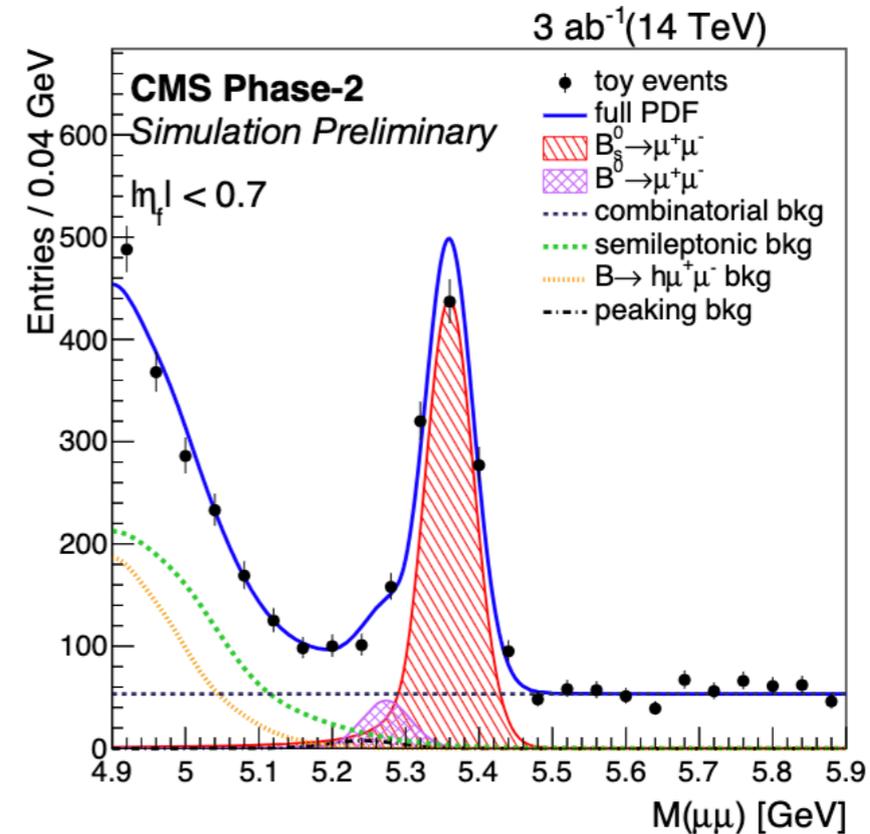
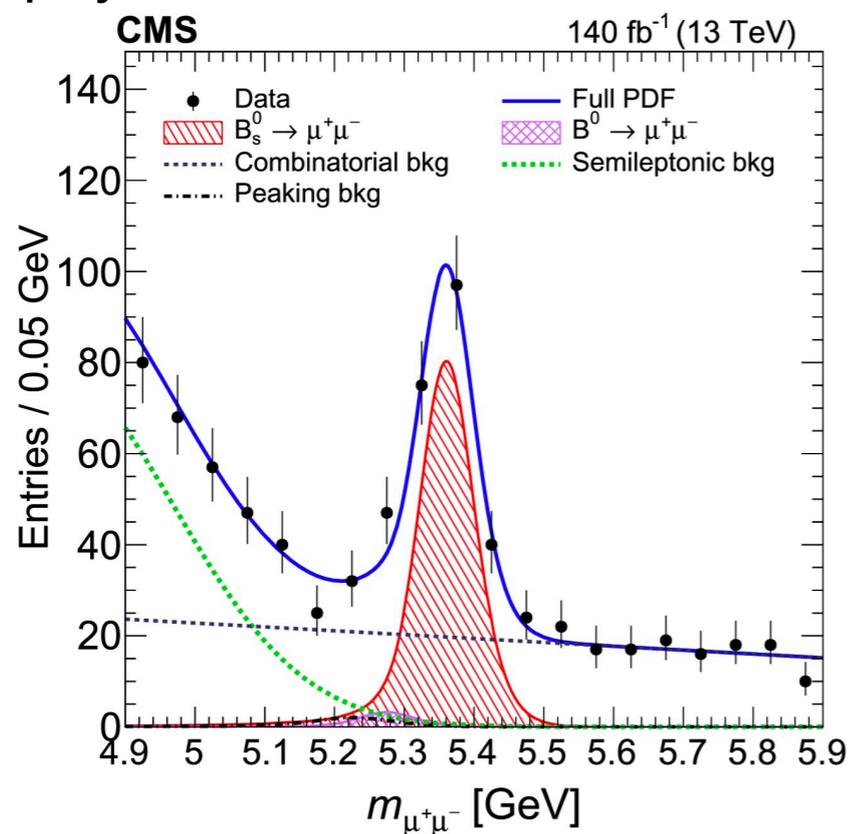
- DT & CSC new FE/BE readout
- RPC back-end electronics
- New GEM/RPC $1.6 < \eta < 2.4$
- Extended coverage to $\eta \approx 3$



Motivations

Physics motivated the general upgrade

- Collect more statistics with better performance to improve measurements and search for new physics



Why do we need a new Tracker?

- Current Tracker sub-detector
 - Is **ageing** and cannot sustain the future radiation doses
 - Low performance/data taking inefficiencies
 - **Designed** for an average **pile-up of 20** need to work with pipe-up 200
 - Higher occupancy, degraded performance (e.g. failure of pattern recognition)

[PLB 842 \(2023\) 137955](#)

[CERN-LPCC-2018-06](#)



Phase2 Tracker

General increase of granularity and radiation hardness

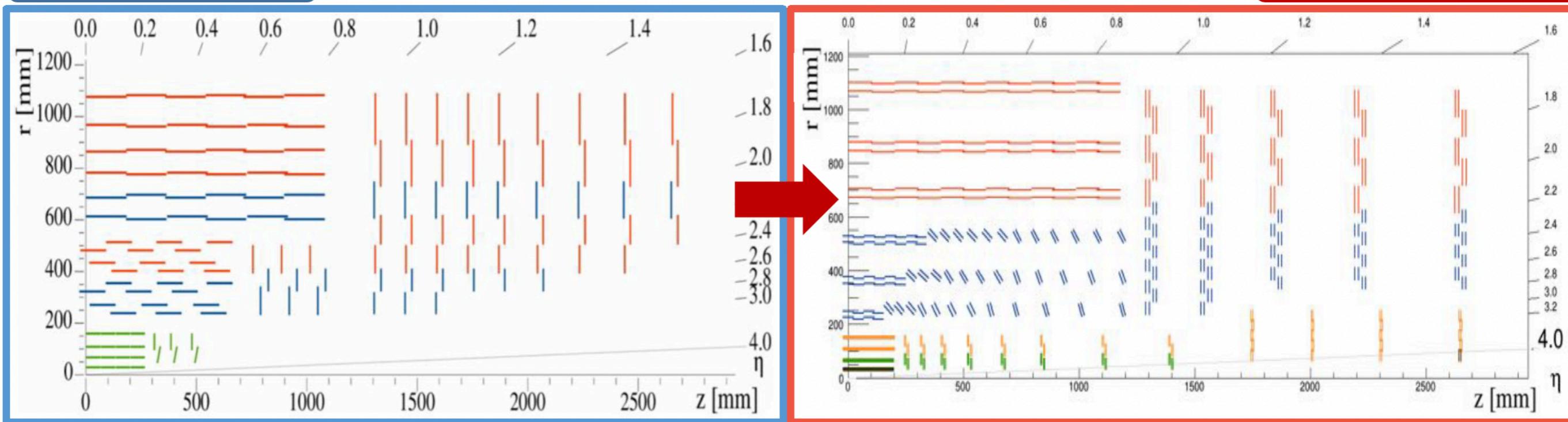
Some key features

- **Tilted geometry** of part of the tracker
- Reduced front-end data rate via in-situ trigger data filtering (**pt modules**)
- Reconstruction of the **charged particle trajectory** at trigger **Level 1** (hardware trigger)

CMS Phase-1 Tracker

CMS-TDR-014

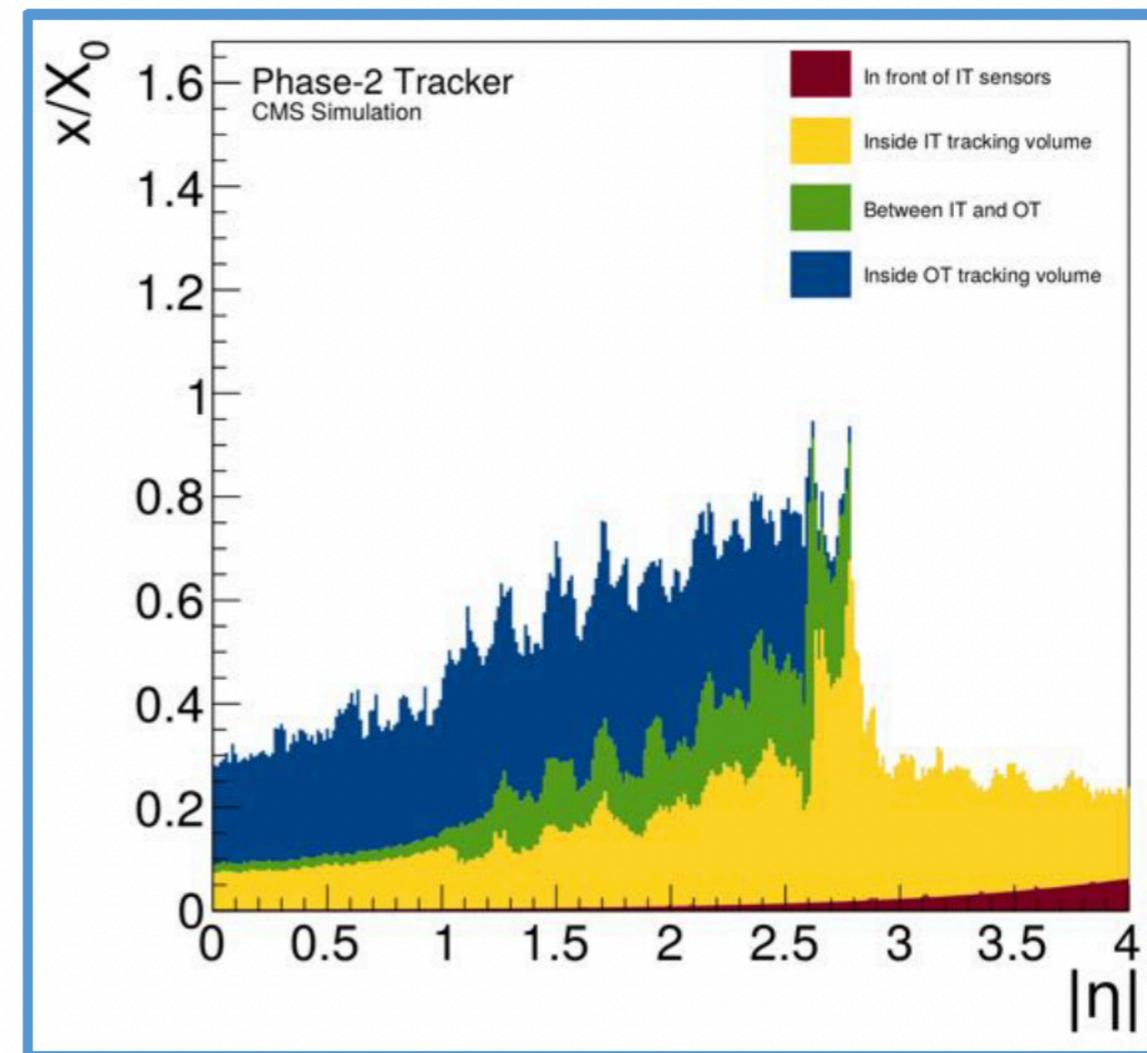
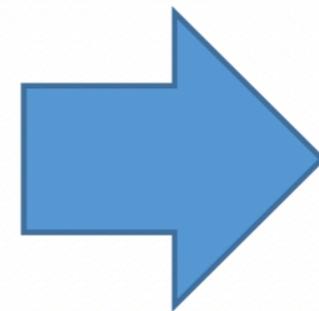
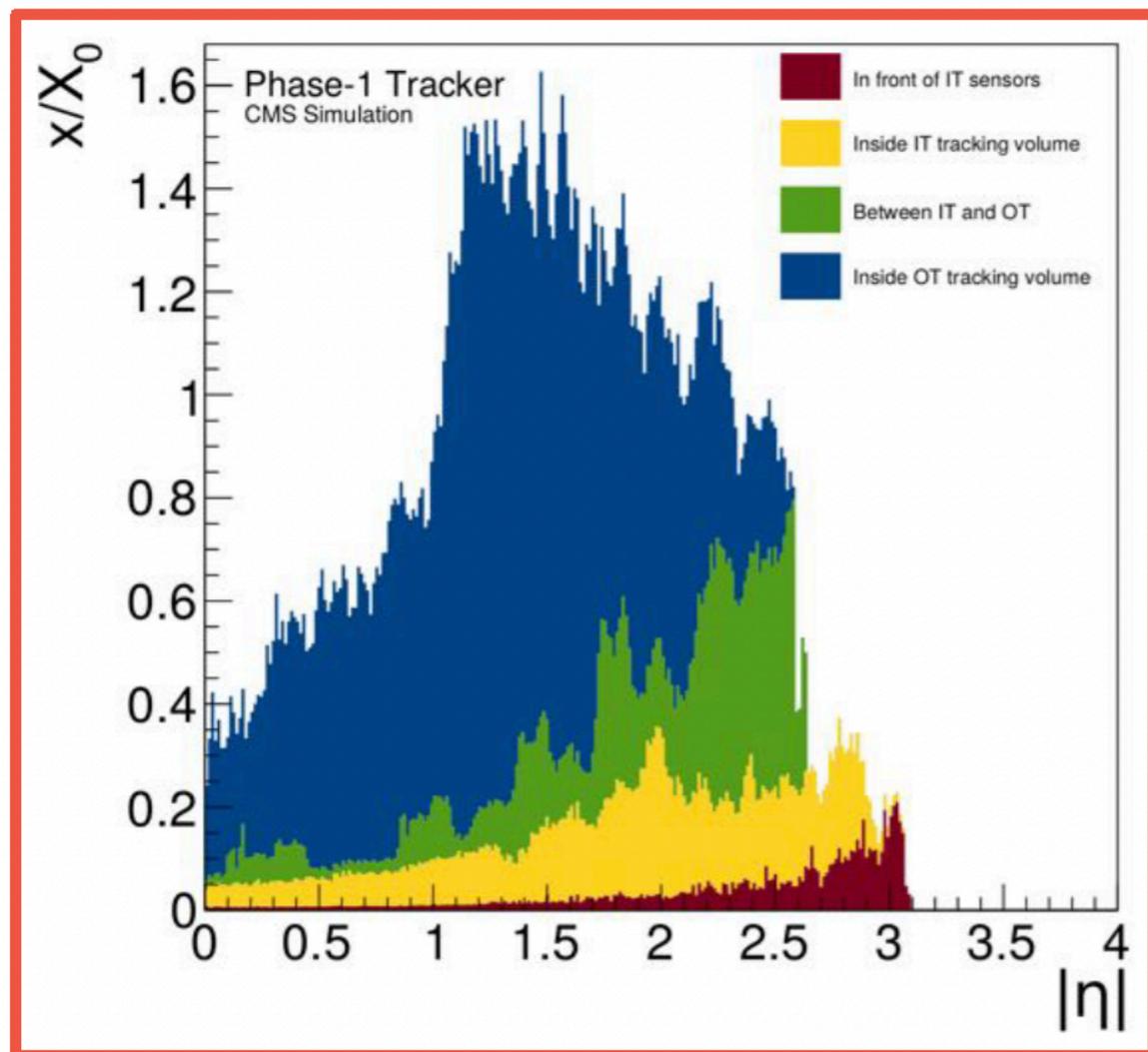
CMS Phase-2 Tracker

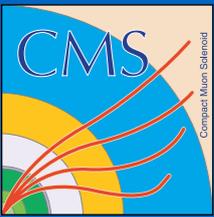


Material budget

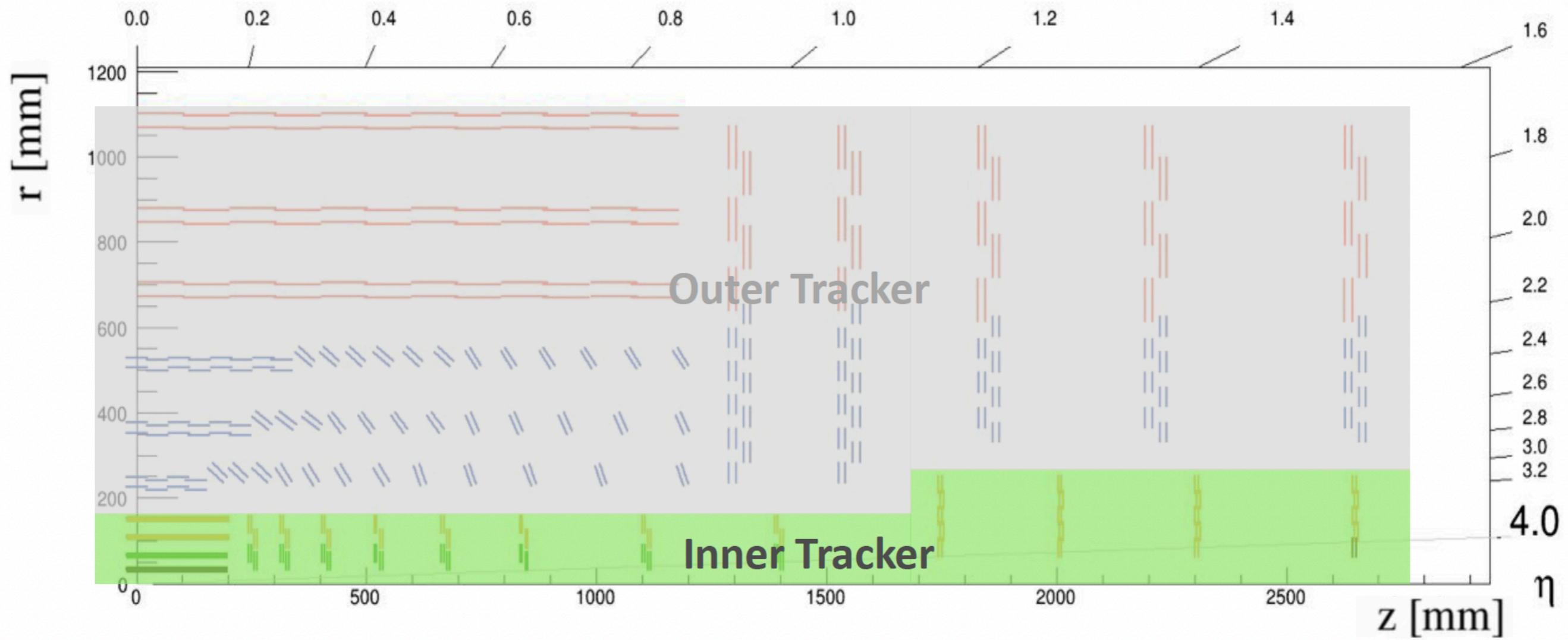
Improvements

- Fewer layers
- Lighter materials
- Optimised service routing
- Tilted geometry
- CO2 cooling





Inner Tracker



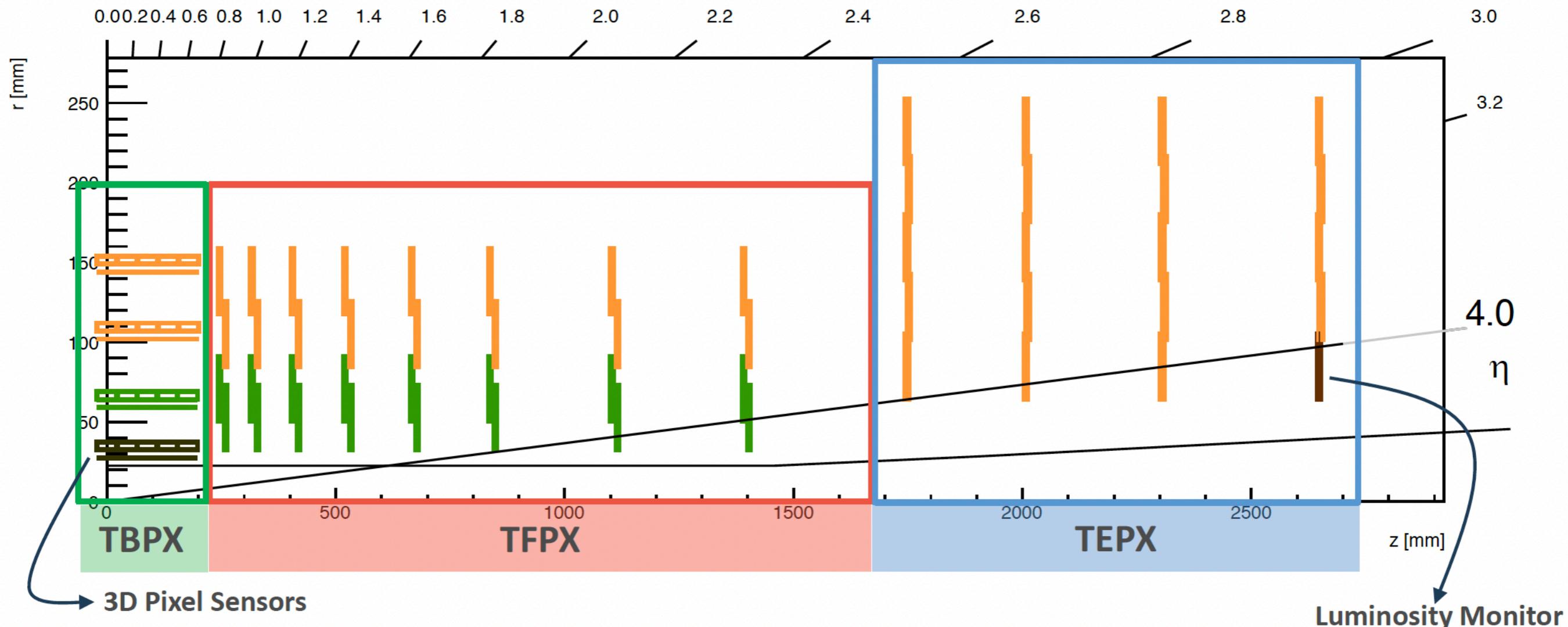


Inner Tracker

Layout

- TBPX : Tracker Barrel PiXeL
- TFPX : Tracker Forward PiXeL
- TEPX : Tracker Endcap PiXeL
- Extended acceptance $|\eta| < 4$ (currently 3)
- Innermost layer at 2.75 cm from beam line (from 2.9 cm)

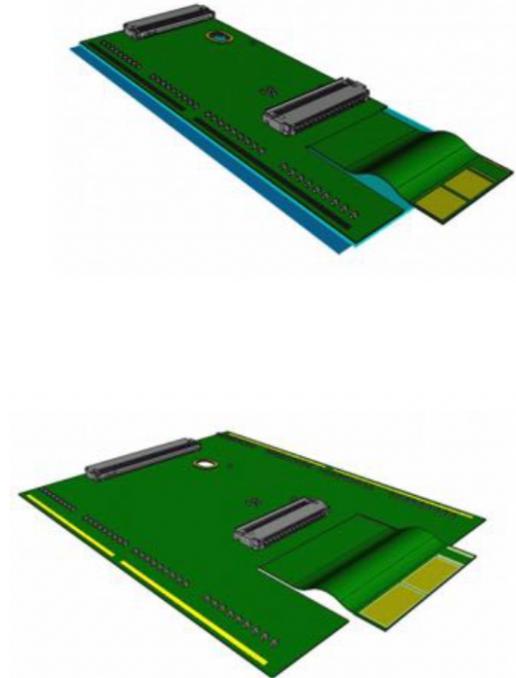
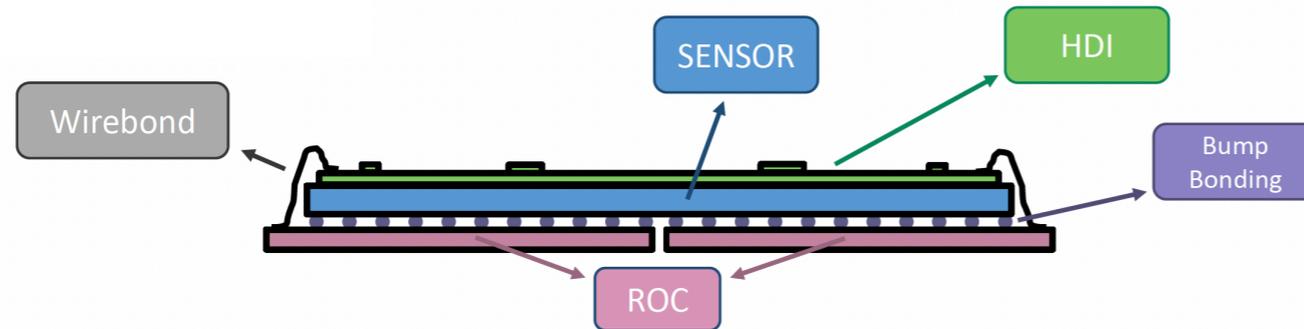
- Designed to be easily replaceable as it will not last up to end of Phase2 (radiation damages)



Inner tracker modules

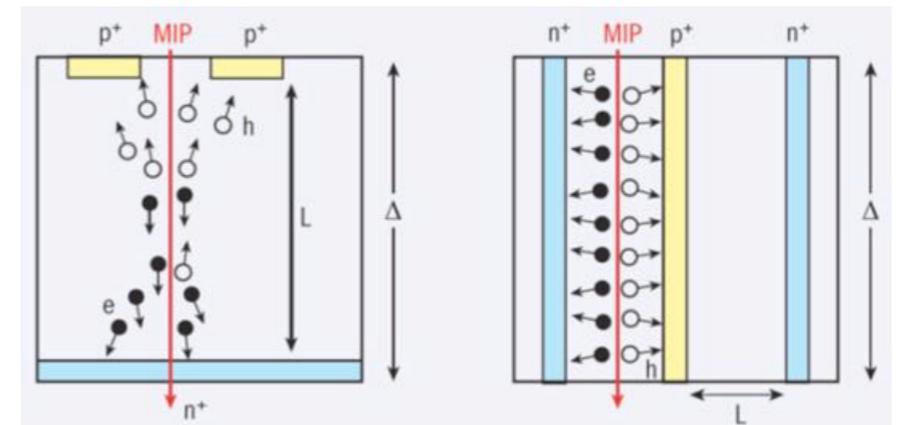
Modules

- Two types of Pixel Modules: 1x2 and 2x2 readout chip
- Read Out Chip (ROC) bump bonded on sensor
- Serial powering scheme with up to 11 modules per chain



Sensors

- 25x100 μm^2 pixel cells with 150 μm active thickness
- Two different technologies will be adopted
 - n-in-p **planar sensors**: hit efficiency >99% after $2 \times 10^{16} n_{\text{eq}}/\text{cm}^2$
 - **3D pixel sensors** on first layer in barrel
 - Less power consumption
 - Stable hit resolution up to $10^{16} n_{\text{eq}}/\text{cm}^2$



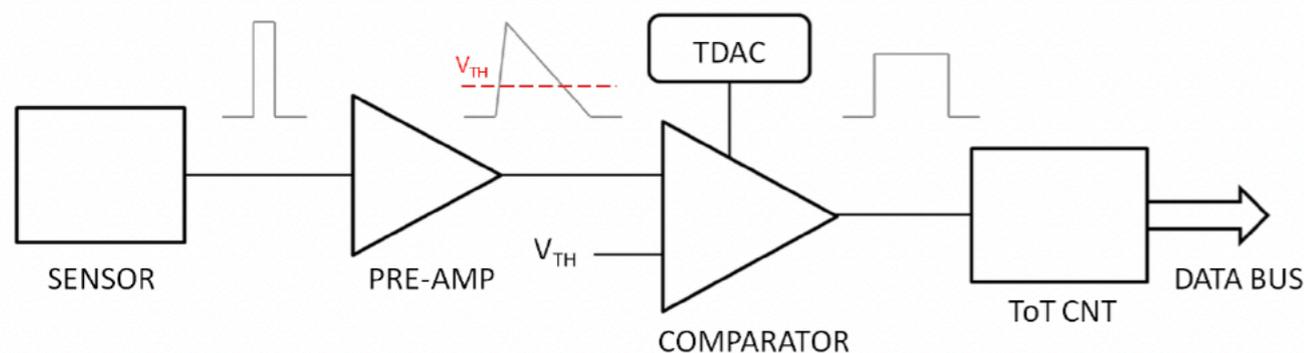
Inner tracker read-out

CERN RD53 ASIC project: $25 \times 100 \mu\text{m}^2$ pixel cells with $150 \mu\text{m}$ active thickness

- Based on CMOS 65nm technology
- Radiation tolerant up to 1 Grad
- Low power consumption $< 1 \text{ W/cm}^2$
- Serial powering via on-chip shunt-LDO regulators

CMS version of RD53 ASIC (C-ROC)

- Full size ASIC: 432×336 channels
- First prototypes modules built with CROC
- Production chip submitted last October





Inner Tracker upgrade in Phase2

Some parts of the Inner Tracker will not survive the entire HL-LHC program

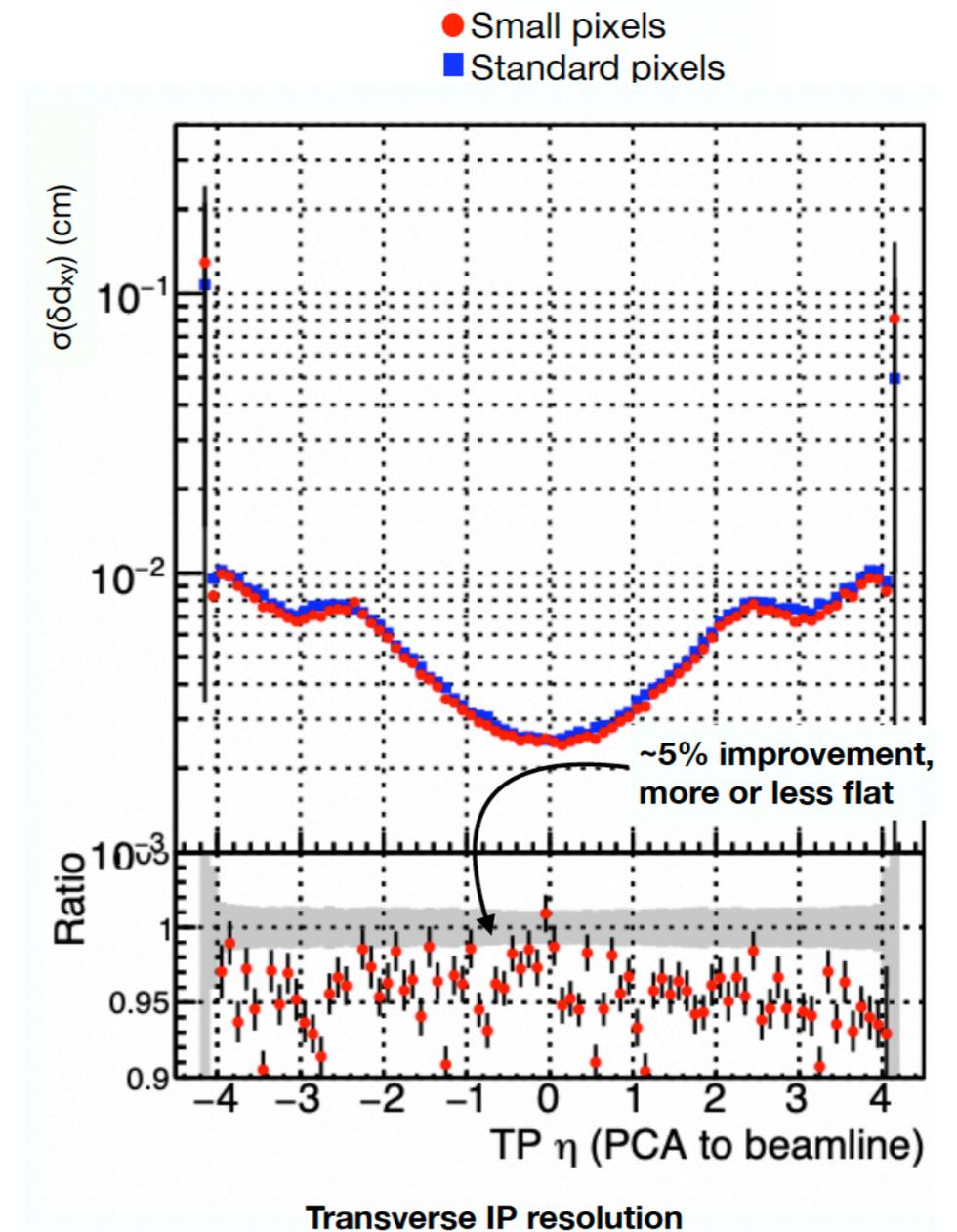
- Discussion has been started to design the replacements
- Possible target for replacement is Run5 of Phase2
- Possible addition of **timing layers** in the end-cap

Preliminary studies

- Assume a pixel reduction size of a factor 0.6
- Sensor thickness 60 μm
- Result: improvements in pixel size brings minimal benefit to tracking **resolution** as it is **dominated by material budget effects**

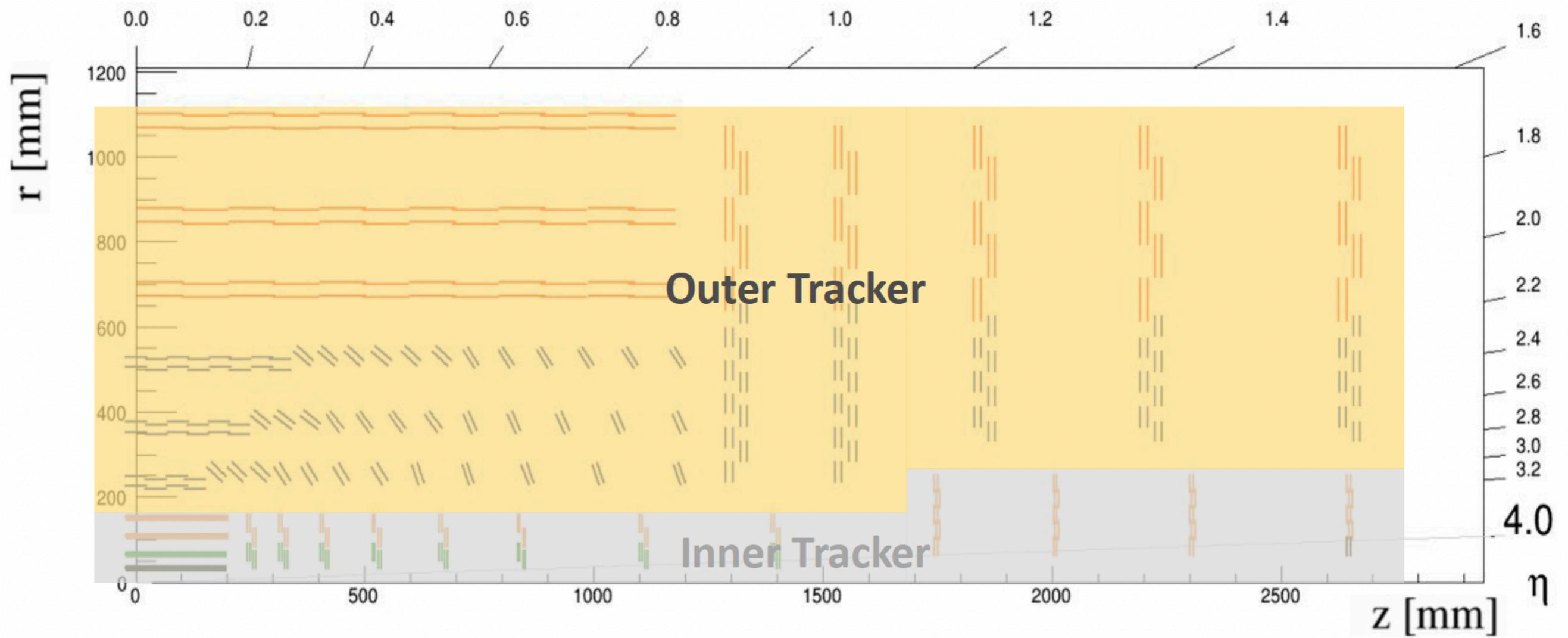
Under evaluation

- Use of **LGAD sensors** for timing modules
- Cooling distribution and cooling contact embedded in mechanical structures





Outer Tracker

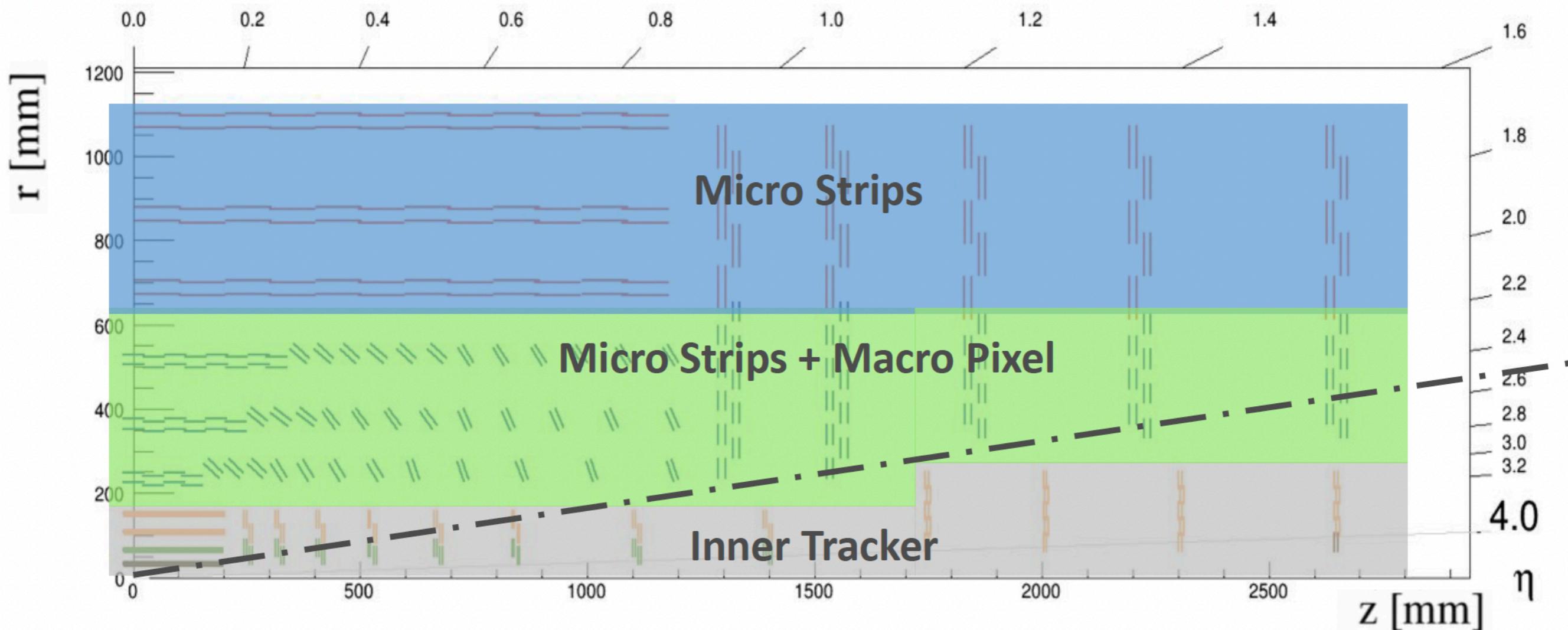




Outer Tracker

Features

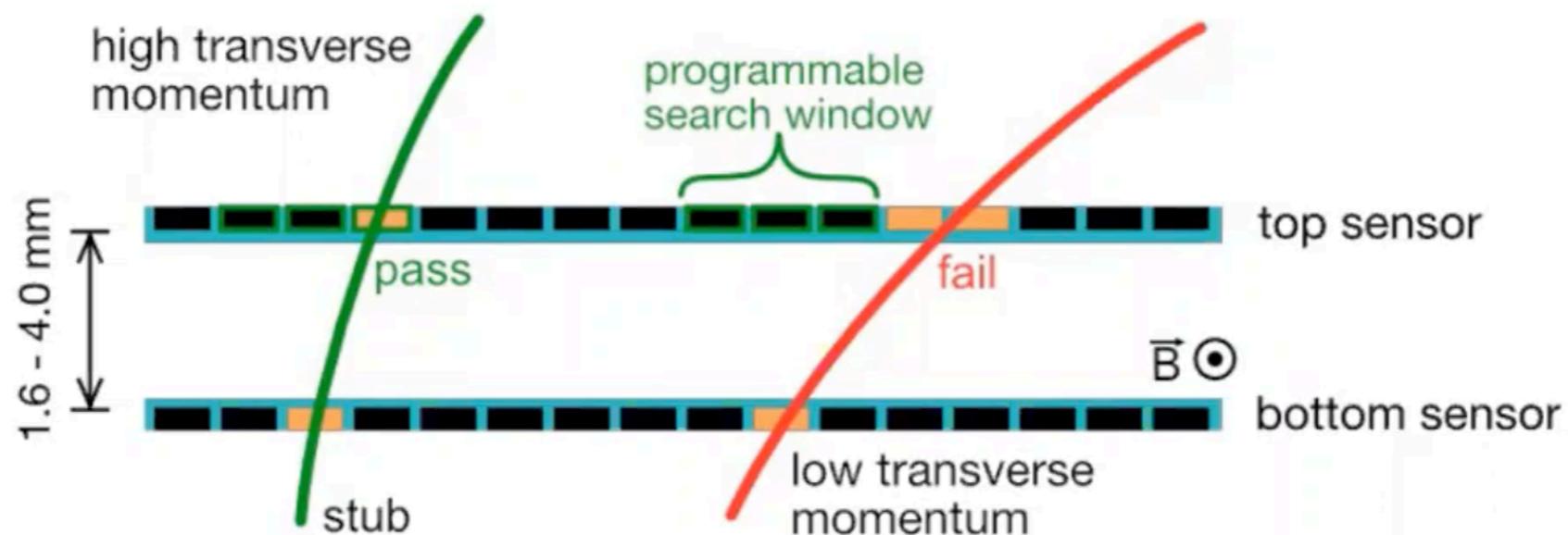
- Two different type of technology: micro-strips and macro-pixels
- Tilted barrel geometry: works better with pt modules, reduction of modules-> decrease of material budget



Pt modules

Pt modules

- **Doublet sensors** with common electronics to **correlate hits** and form **stubs** for trigger
- Distance between sensors give track pT lower cut
- Allows control of **trigger data rates** (reduction of a factor 10) and hugely improved pT resolution
- Different sensor spacing for different detector region

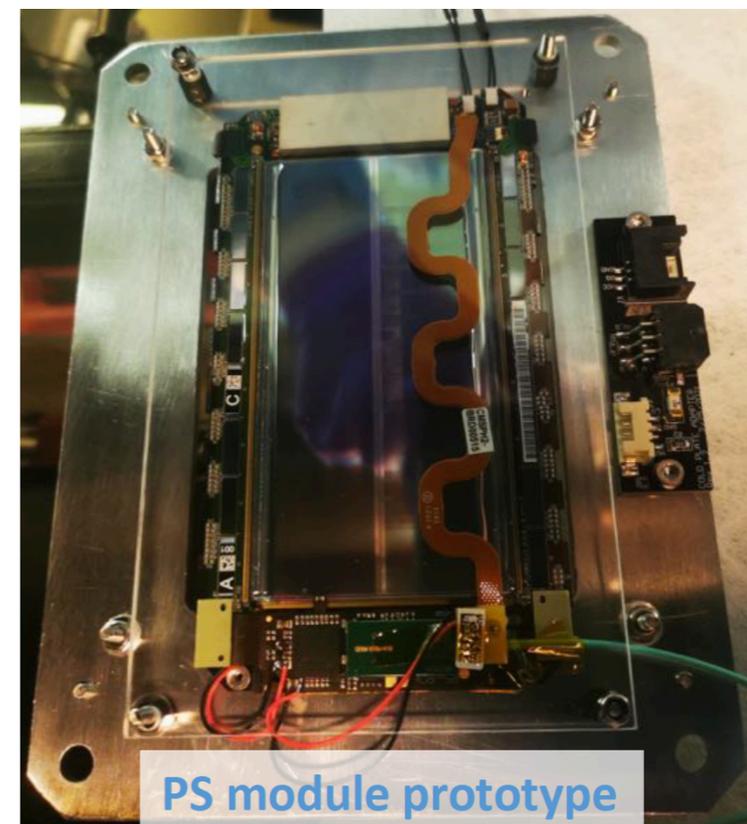
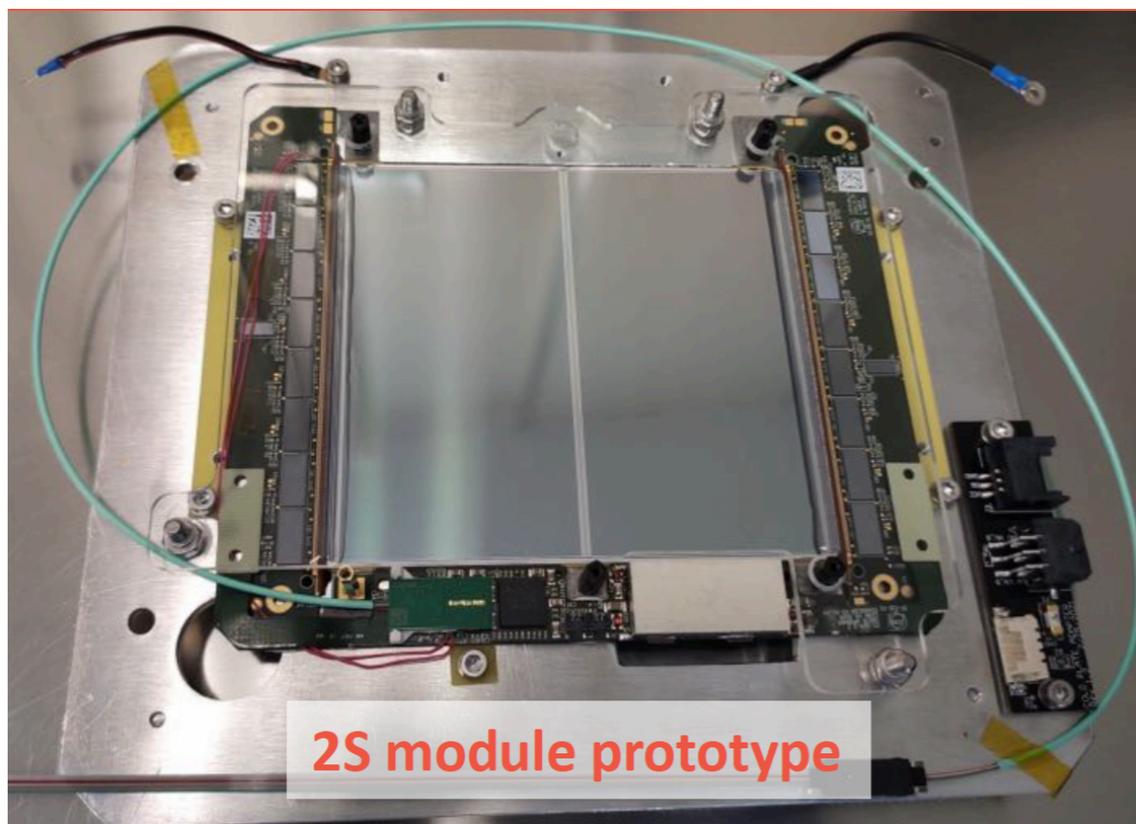


Outer Tracker Modules

Two module types

- 2S modules of 10x10 cm²
 - Two different spacing : 1.8mm and 4mm
 - Two micro strip sensors with 5cm x 90μm strips
- PS modules 5x10 cm²
 - Three different spacing : 1.6mm, 2.6mm, and 4mm
 - One strip sensor: 2.5cm x 100μm strips
 - One macro pixel sensor : 1.5mm x 100μm pixels

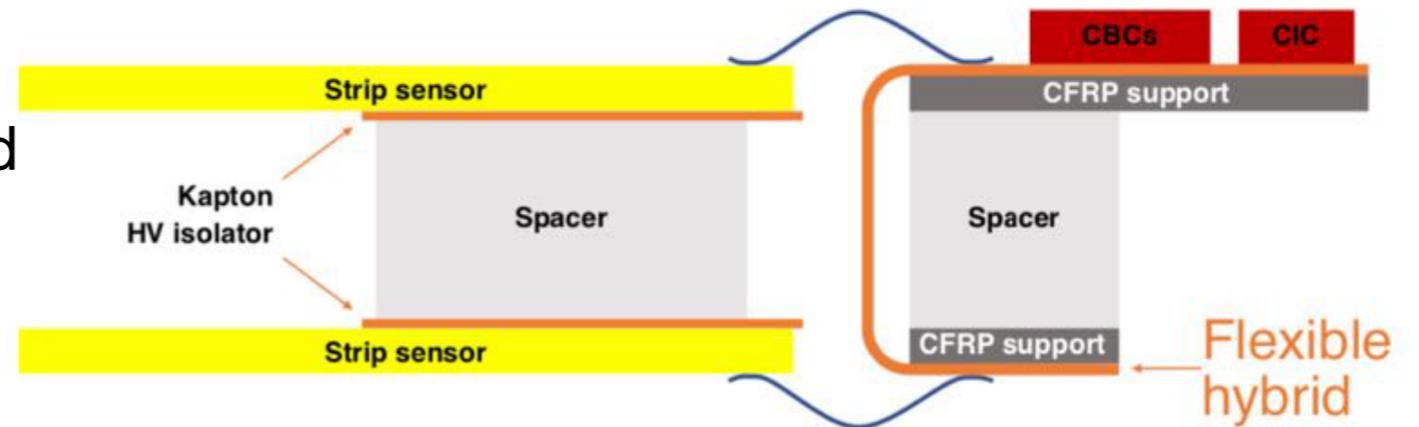
Prototypes already used for testing since 2022, pre-production modules by the end of 2023



Outer Tracker read-out

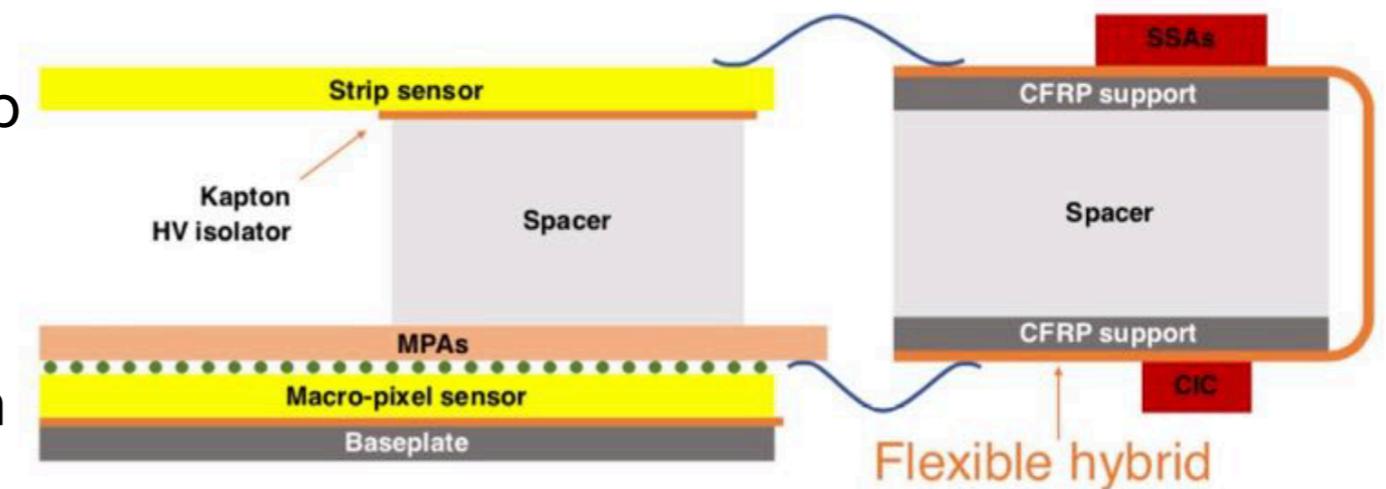
2S Module ASIC (130nm)

- CMS Binary Chip (CBC) for readout and stub finding for L1T
- CBC reads out both sensors
- 254 channels per chip



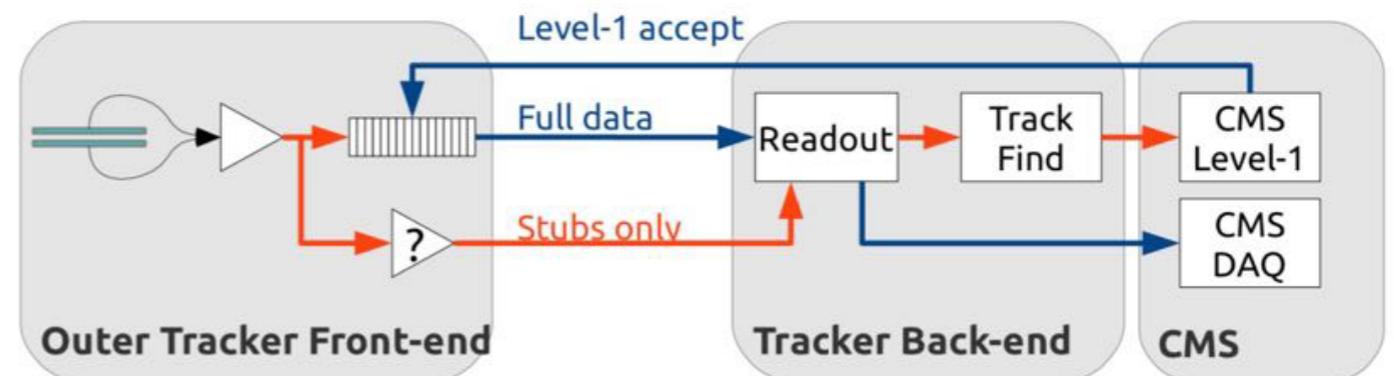
PS Module ASICs (65nm)

- Macro-Pixel ASIC (MPA) and Short-strip ASIC (SSA) for readout of sensors
- Stub finding performed by MPA
 - SSA sends cluster and L1 information to MPA to enable match in space and time



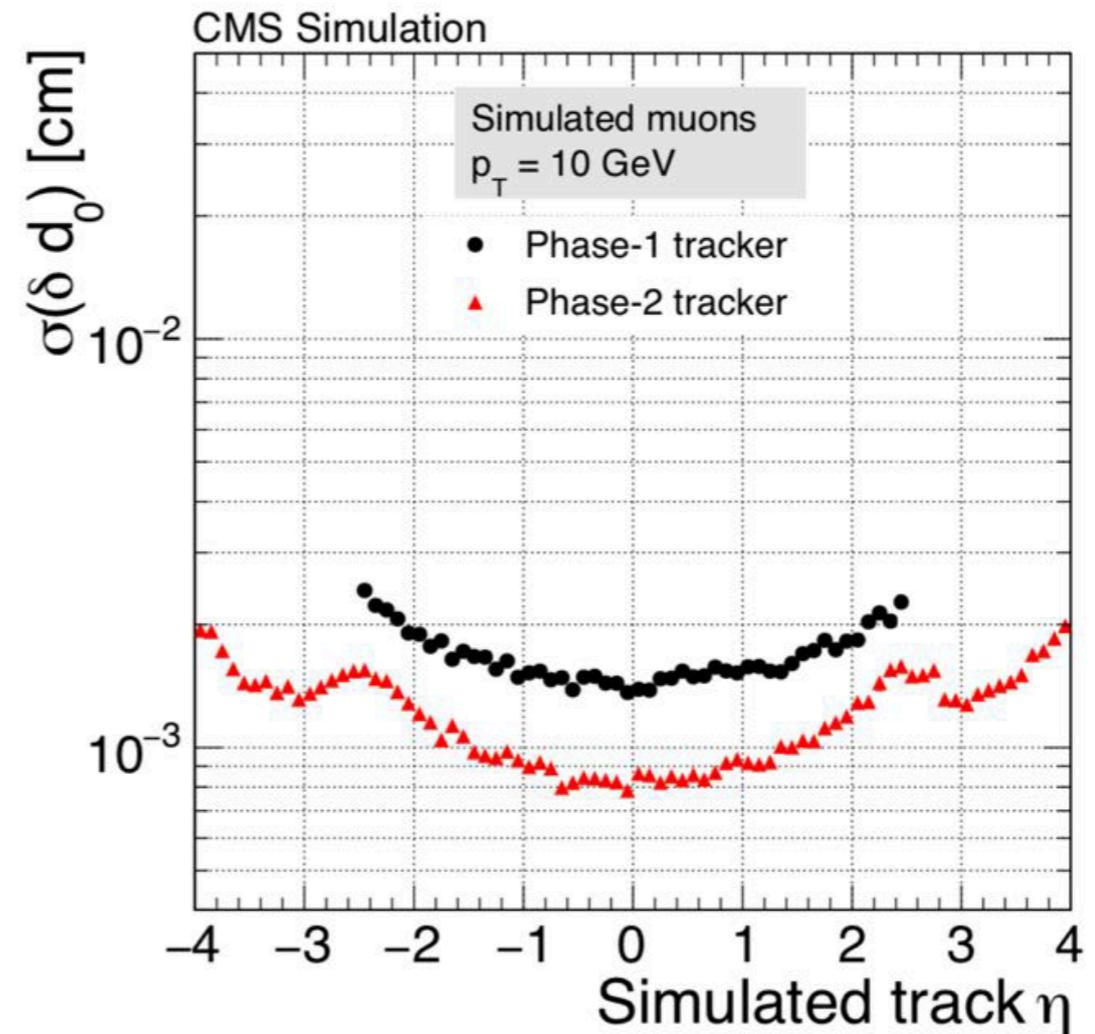
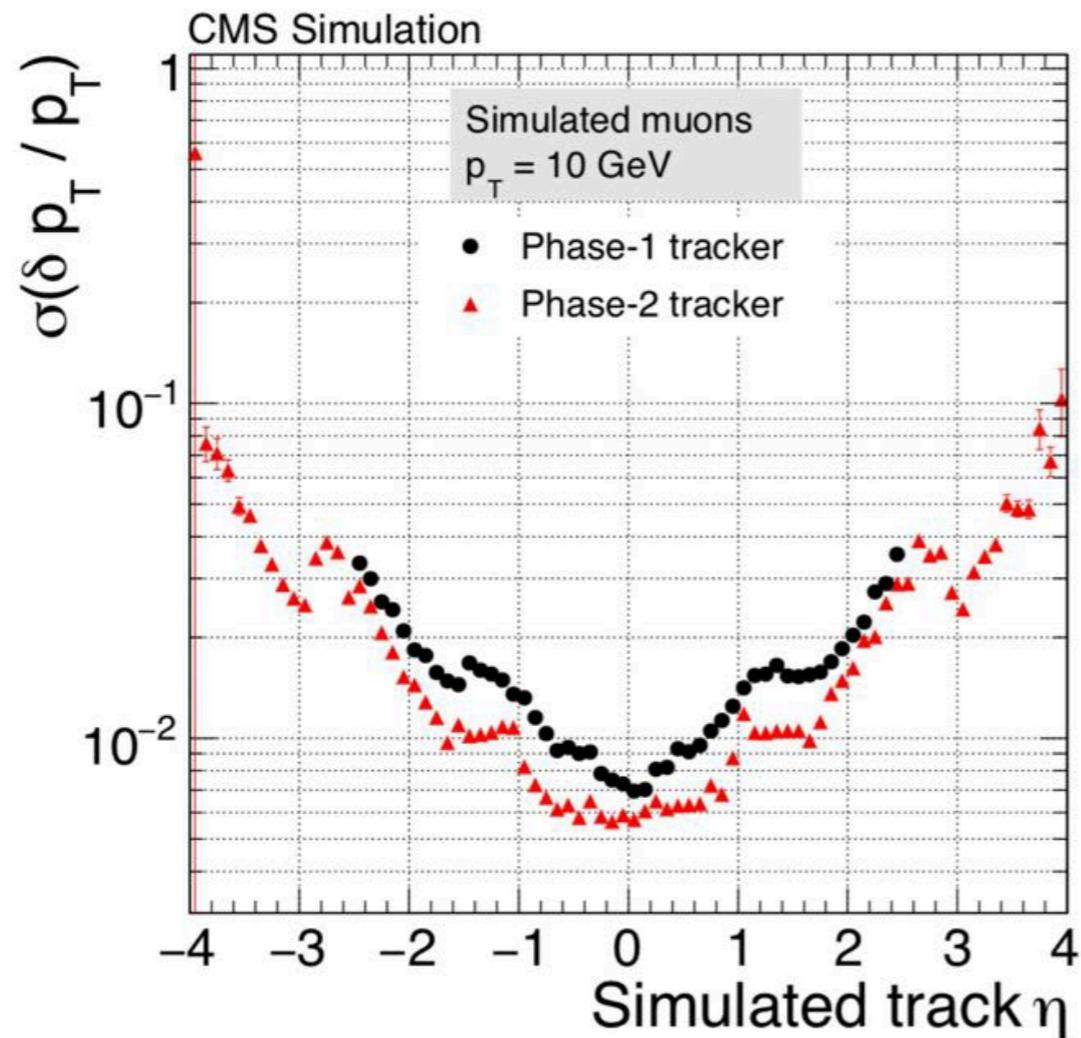
Common ASIC (65nm)

- CIC concentrator chip
- Receives L1 information and readout data



Performance: tracking resolution

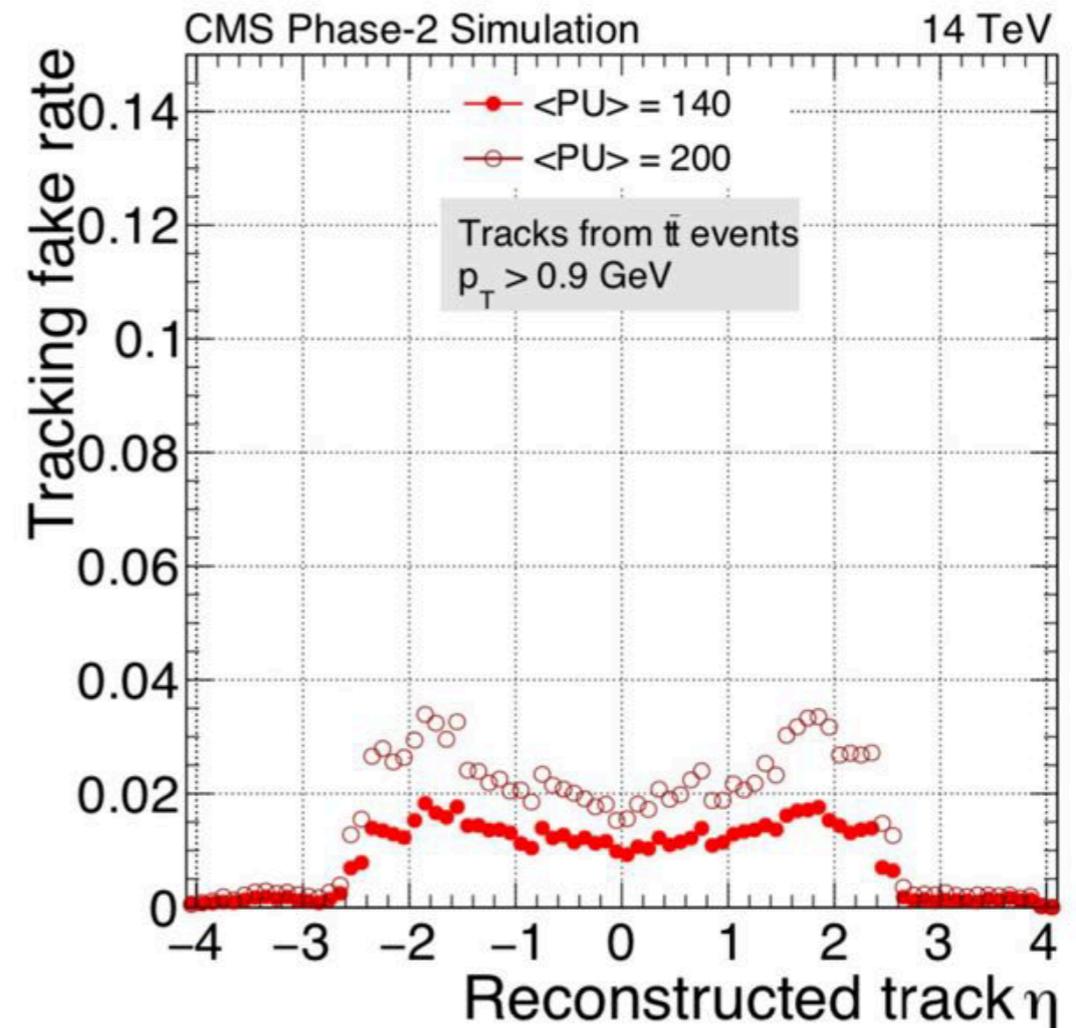
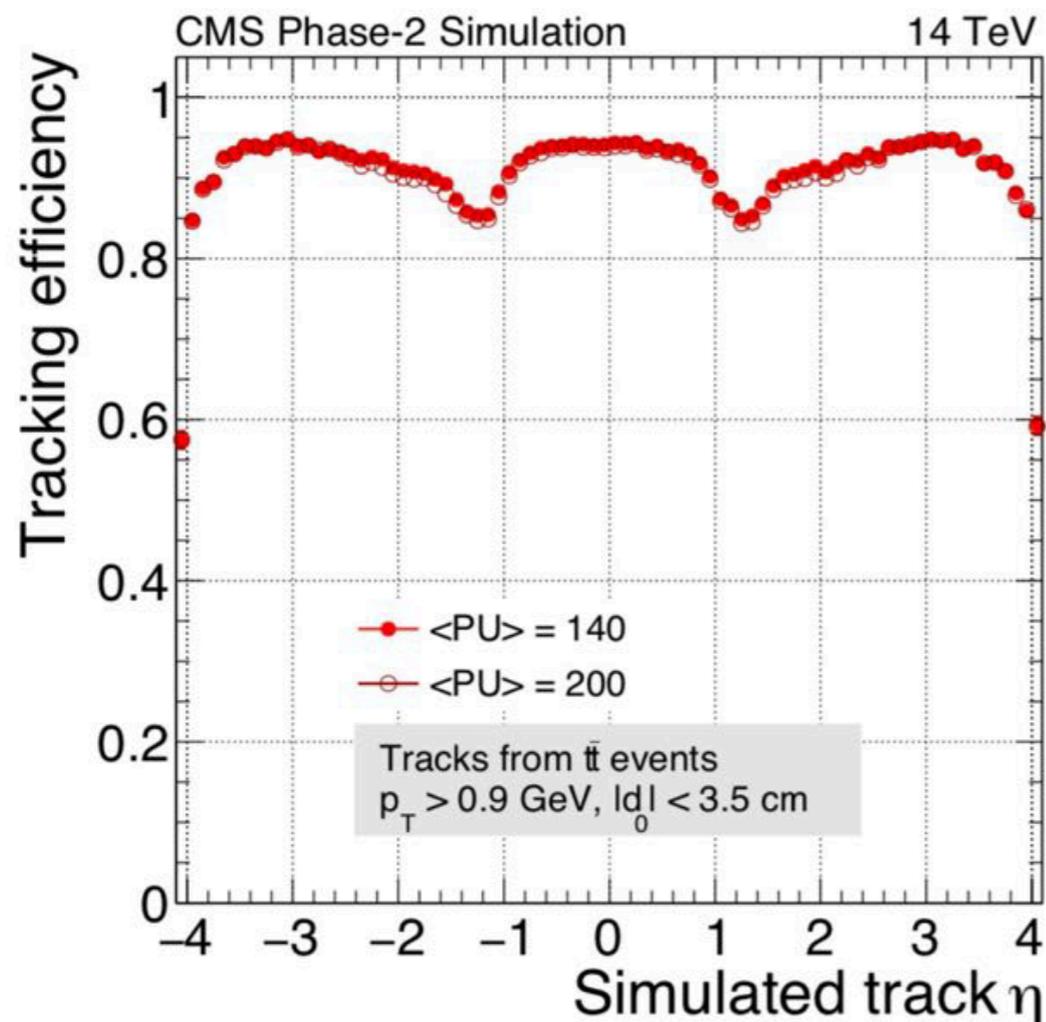
Better momentum and impact parameter resolution





Performance: pile-up dependence

- High tracking efficiency and low pile-up dependence (deeps are transitions in inner tracker)
- Fake rate below 2% at PU 140, small defence on pile-up



Back-end

DTC: Data carrier

TFP: Track Fitter

DTH: Clock & Trigger distribution + Data carrier



Trigger Data – 40MHz
L1A Data – 750kHz

Front-End
5G-10G

Outer Tracker DTC Board
(Serenity)



Trigger Data
Back-End
25G

L1A Data
DAQ
25G

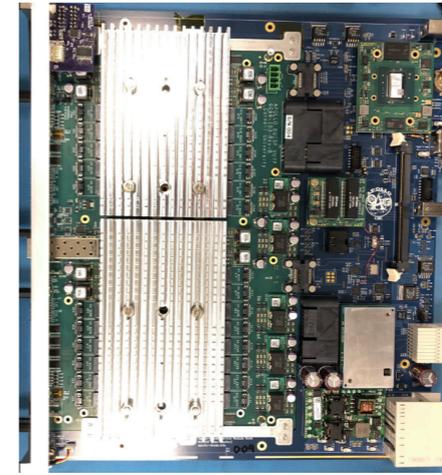
L1A Distribution
TCDS2

Inner Tracker DTC
(Apollo)



DAQ
L1A Data

TFP Board
(Apollo)



DAQ
L1A Data

DTH Board



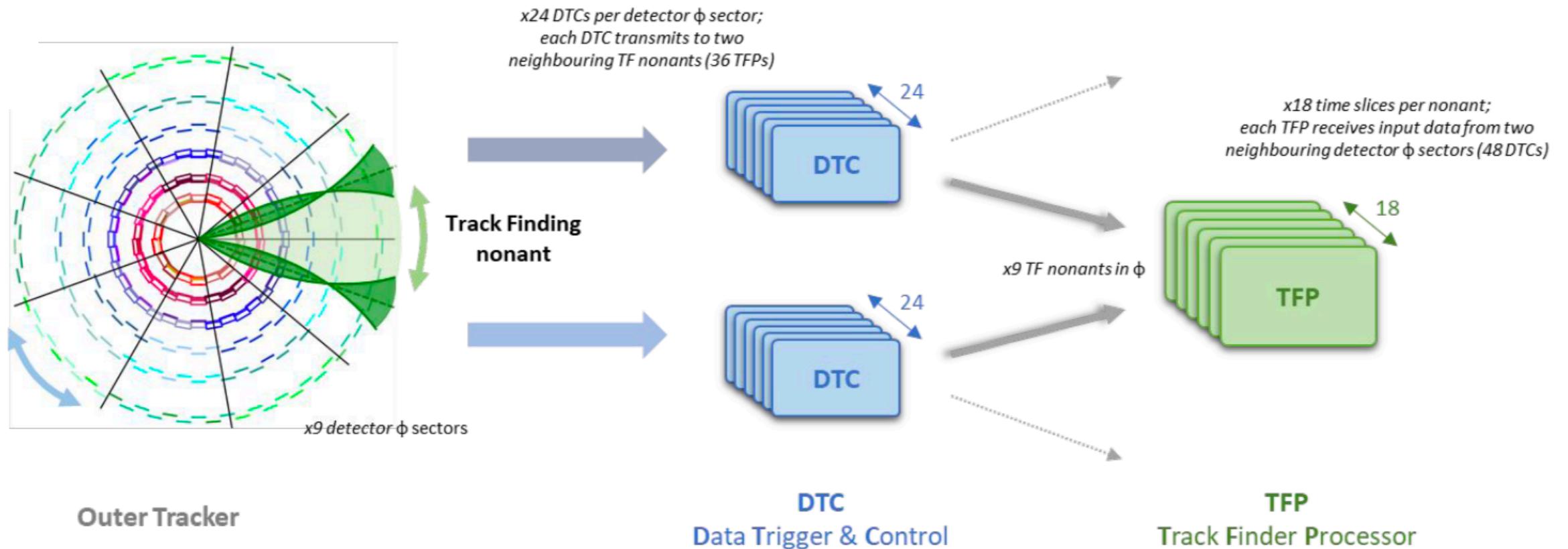
DAQ

DAQ
HLT – High Level
Trigger



Prototype ATCA boards

Track Trigger



Track reconstruction at trigger Level 1 in less than $4 \mu\text{s}$

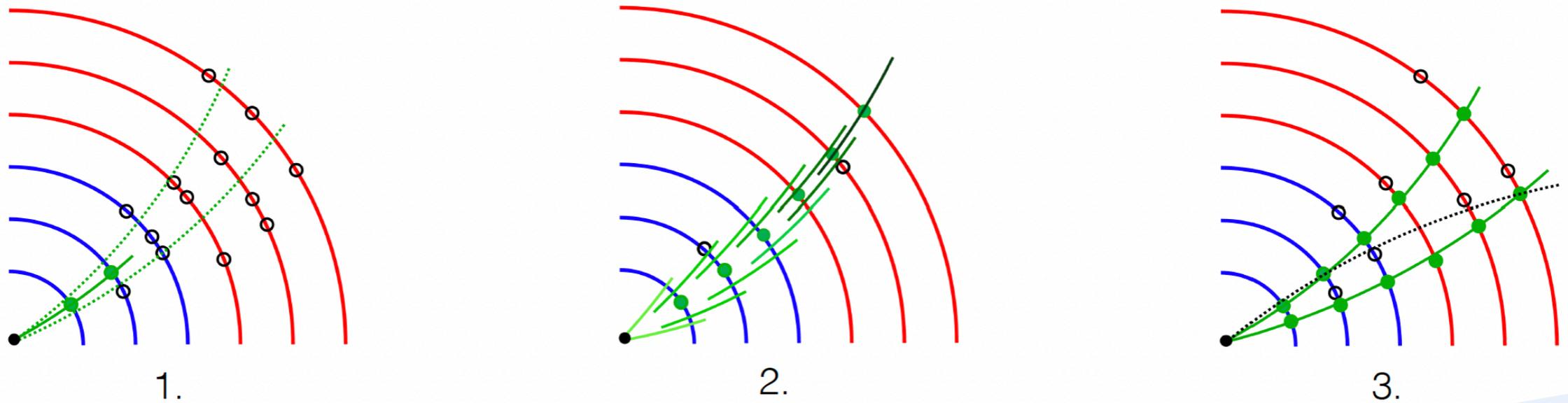
- Data from outer tracker in $|\eta| < 2.4$ are sent to DTC, which sends the data to TFP with a time multiplexing of $\times 18$
- Each TFP board receives an event every 450 ns

Track Trigger Algorithm

Each event could have 10k stubs and $O(100)$ reconstructed tracks \rightarrow harsh combinatoric problem

Algorithm under development: Tracklet + Kalman filter

1. Pattern based on tracklet seeding
2. Kalman filter for identify best stub candidates and track parameters
3. Boost decision tree to evaluate track quality



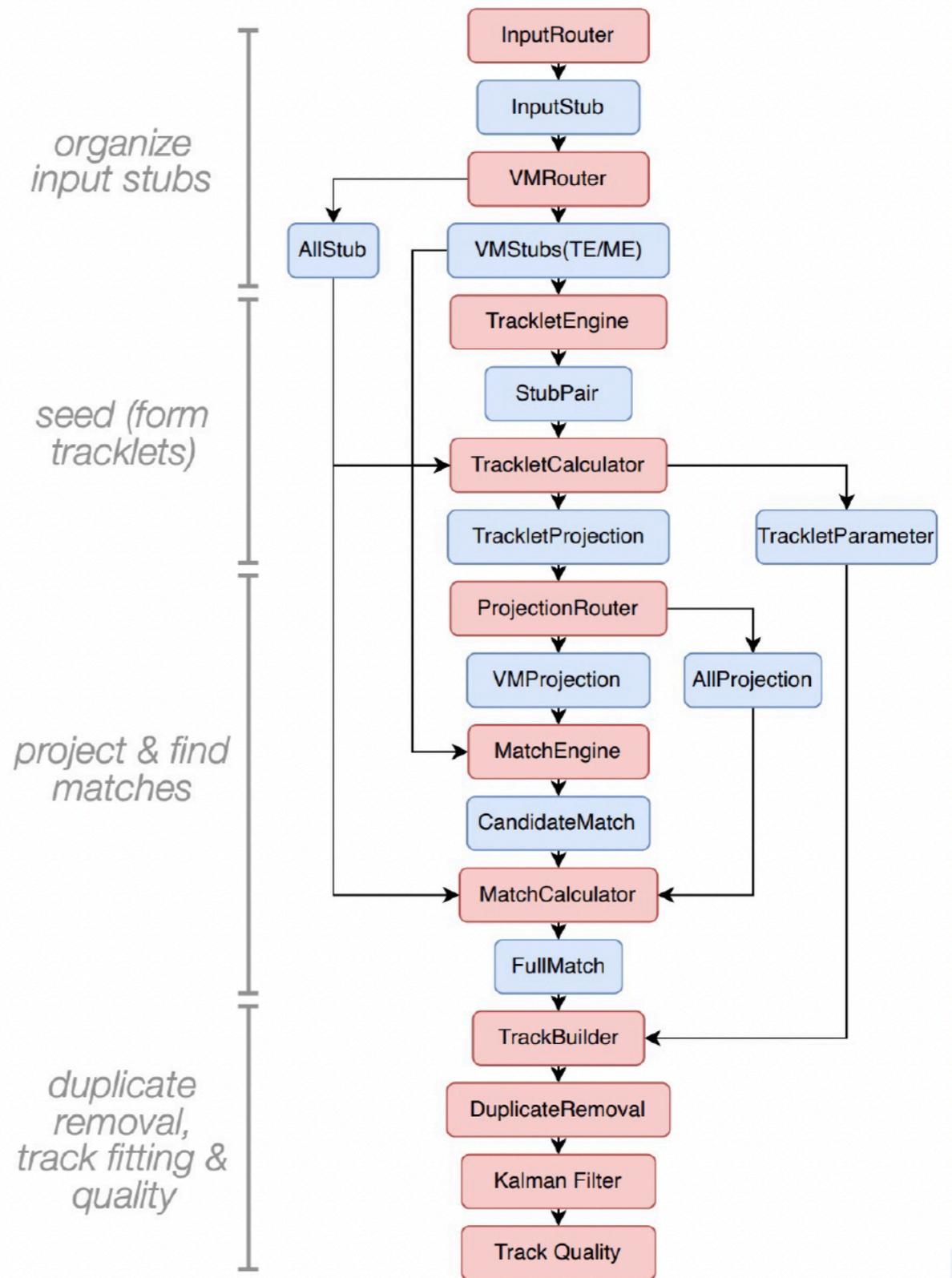
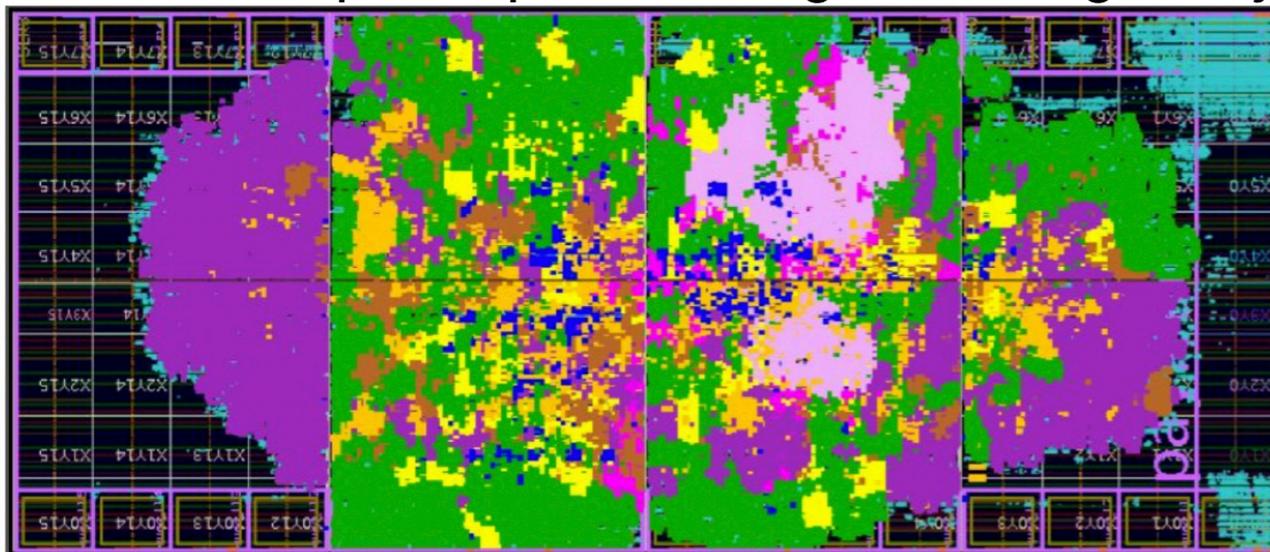
Track Trigger Algorithm Firmware

- Implemented in HLS and VHDL in FPGA
- Pipeline made of processing modules (red) and memory modules (blue)
- Horizontal scalability (**parallelisation**)
- Kalman filter and Track quality written in VHDL
- Targeting 240 MHz

Status

- All modules ready
- Full algorithm needs two VU13P FPGA
- Still under **optimisation**

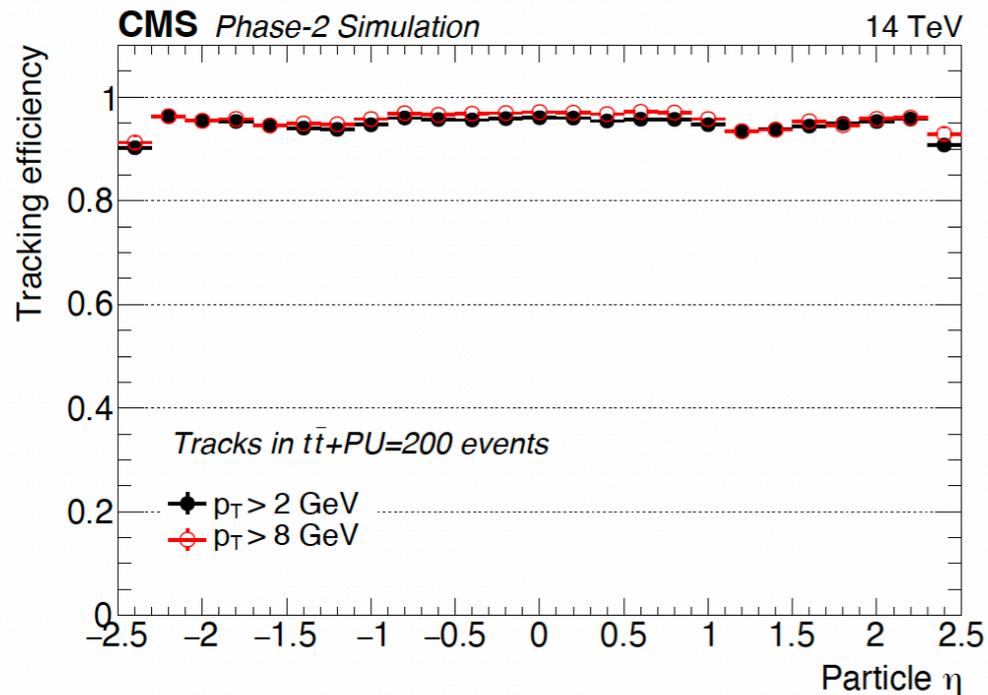
VU13P floorplan - patten recognition stage only





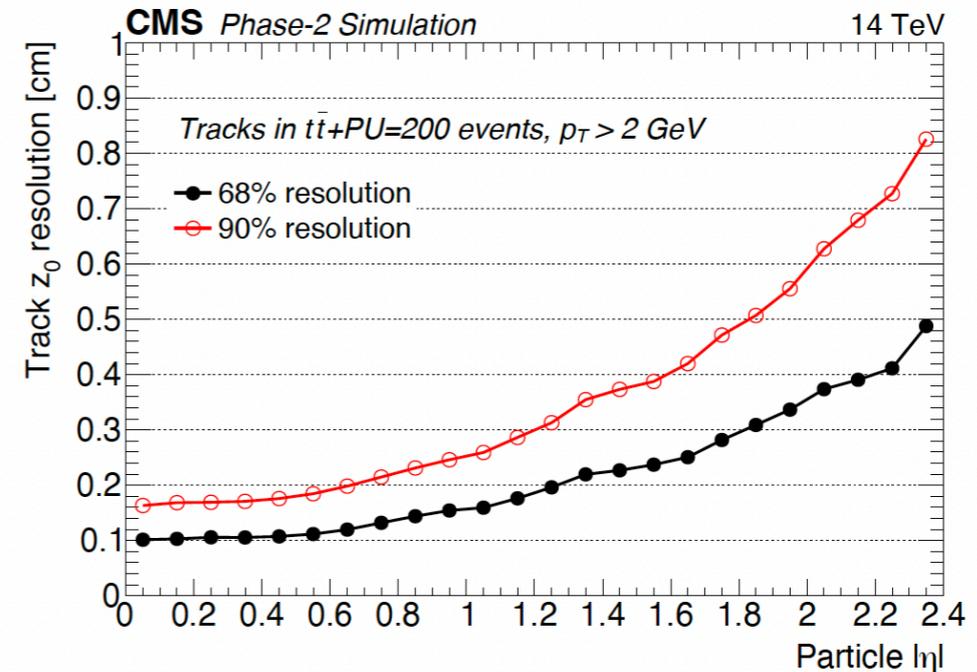
Track Fitter Performance

High efficiency across η

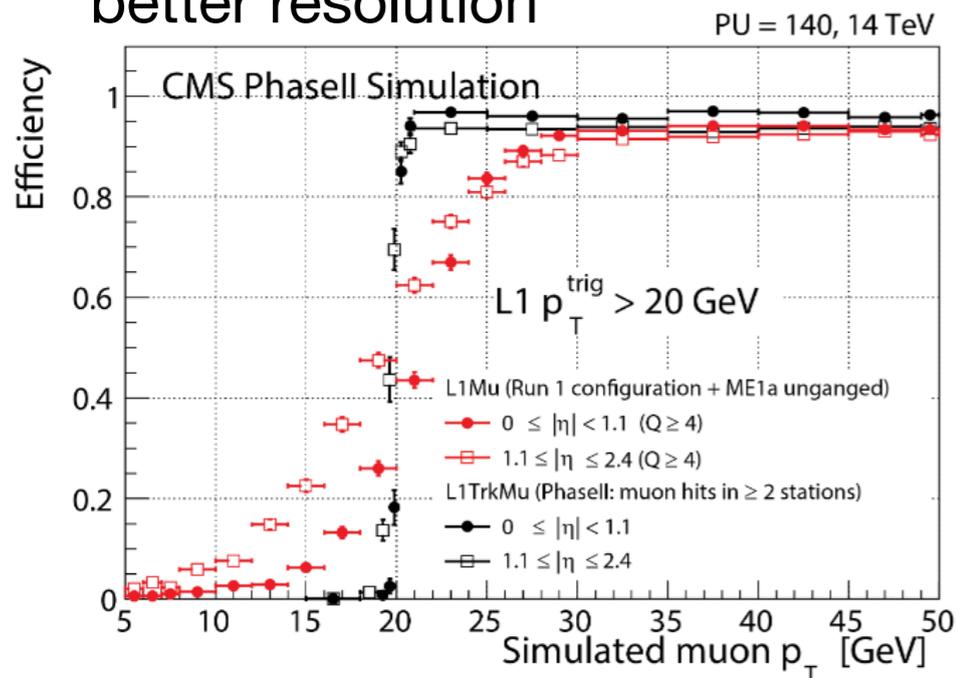


1 mm z_0 resolution for tracks

Enough for vertexing at Level 1 Trigger

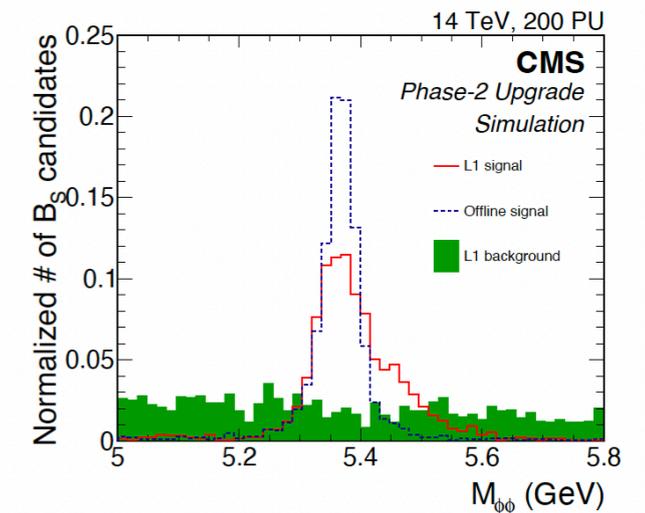
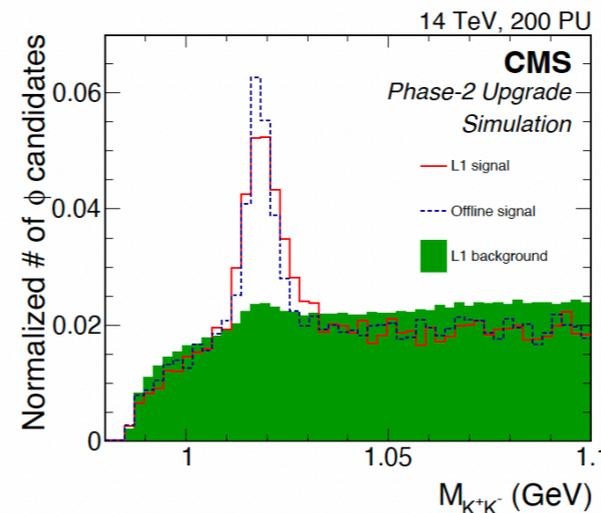


Muon L1 reconstruction: better resolution



Access to hadronic channels:

e.g. $\phi \rightarrow KK$ and $B_s \rightarrow \phi\phi$



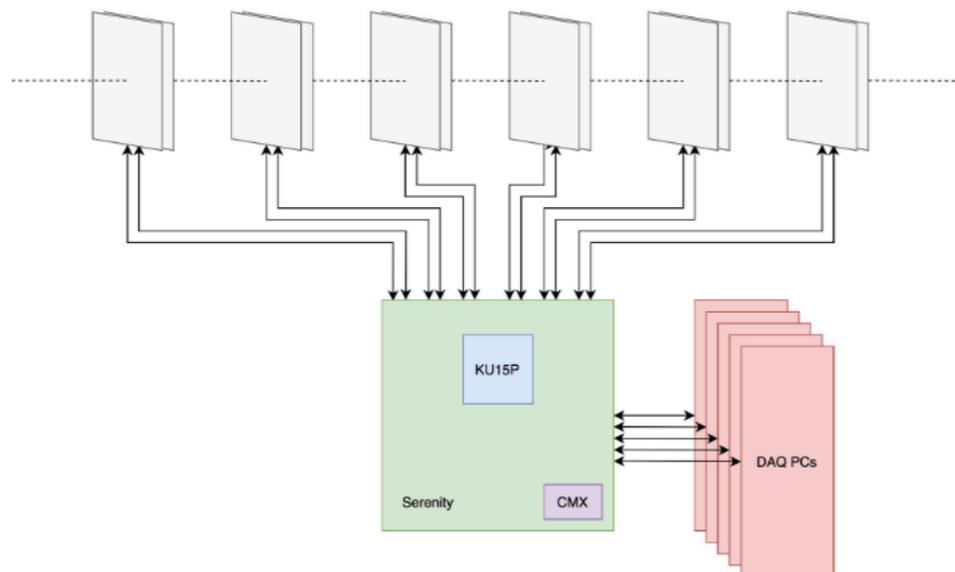
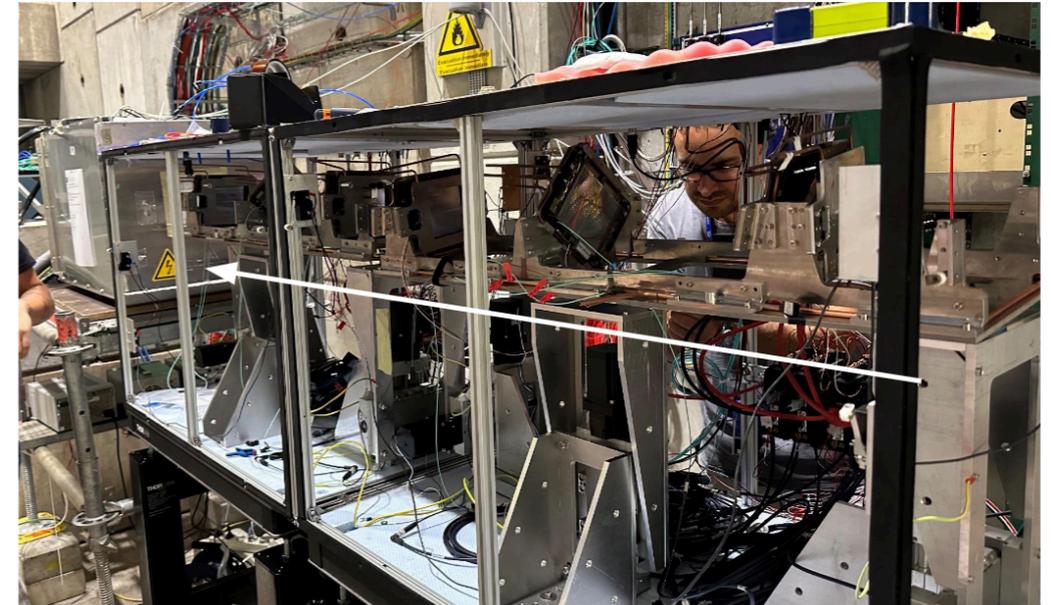
Vertical slice: test beam

Test beam with 160GeV muon beam

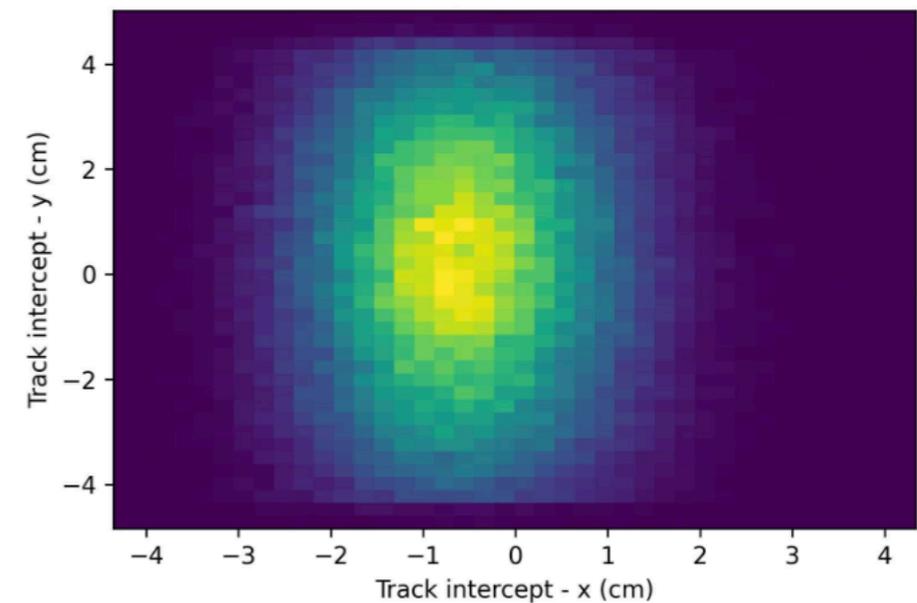
- Multiple session of tests carried out in 2022 and 2023
- **Latest beam test done with 12 2S modules**
- Vertical slice: from front-end modules to the data carrier board (DTC)
- 40MHz readout of stubs

Test results

- **5 trillion stubs** collected
- Stable for many hours
- **Module synchronisation** (within 1ns) and efficiency plots
- Data analysis is ongoing

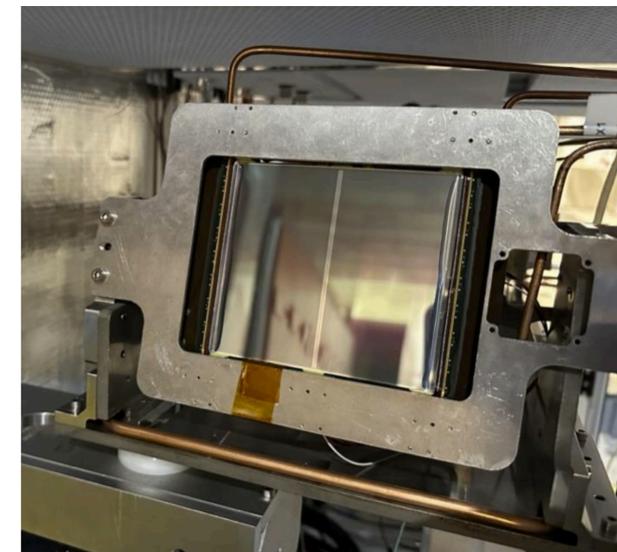
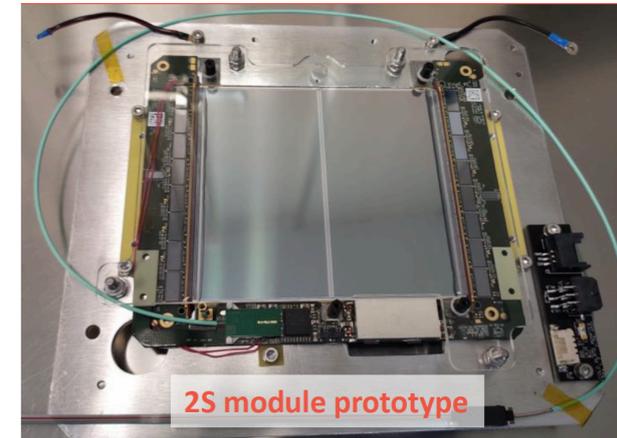


Beam spot: x vs y



Conclusions

- The Tracker sub-detector of CMS will be replaced before the Phase2 starts
 - **Outer Tracker** made of strip and pixel/strip sensors
 - **Inner Tracker** made of pixel sensors
 - Some parts need to be **replaced** during Phase2, discussion on how to do it is ongoing
- **Tracking at Level 1** will be implemented for the first time in CMS
 - Great benefit in term of trigger threshold selection and pile-up rejection
- **Prototypes** of modules and back-end boards have been **successfully tested** standalone and in slice tests
- In **2024** we start the **production** of the final modules and back-end boards looking forward the start of Phase2 in 2029



Additional slides